Fall 2015

ENEE 2586

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University of New Orleans

ENEE 2586-001 Logic Circuits Laboratory Fall 2015

Syllabus

Learning Objectives: After successfully completing this laboratory course, students will be able to design, analyze, and implement digital logic circuits.

General Description:
The circuits lab contains selected experiments and projects to accompany the lectures of ENEE 2582.

Prerequisites: ENEE 2582 Digital Logic (co-registration)

Instructor: Dr. Huimin Chen, Associate Professor
Office: EN-819 Tel: 280-1280 Email: hchen2@uno.edu
Office Hours: Monday 1:00pm – 3:00pm or by appointment

Assistant: TBD

Laboratory Hours: Monday 9:00am – 11:45am, EN 713

TOPIC	WEEKS
Introduction to basic logic chips and test equipment	1
Combinational logic circuits	2
Kmaps and arithmetic operations	2
Multisim simulation of logic circuits	1
Flip-flops	1
Counters	1
State machines	1
Design project	2

Grading Policy

Pre-lab circuit design	10 %
In-lab performance	15 %
Written Reports	60 %
Final Project Presentation and Report	15 %

Attendance: Attendance is mandatory and will be recorded. Predicted absences must be approved in advance.

Written Reports

Each student must submit a report written **individually** that shall be typewritten with pages (except cover) numbered. Turning in exact copies of someone else's lab reports is not acceptable. The reports will be graded based on the following criteria: proper section, neatness, clear presentation, explanation of experimental data, comparison with the logic circuit analysis results, sensible discussion and conclusions. Lab reports are due at the **beginning** of the class of the week following each experiment. There will be a 10% penalty (for each day) for late report.

Reports must include at a minimum of the following sections:

1. Cover page – Show the course number and section, instructor name, title and date of the experiments, experiment number, student's name and lab partners.
2. Objectives – States the objectives of the experiments and briefly describe the scope of the experiment.
3. Equipment – List of equipment used (including brand and model).
4. Theory – Discuss the circuit theory involved in the experiment, including all formulas used, circuit diagrams (should not be free hand drawings). Number all equations.
5. Procedure – Write down a step-by-step procedure of the performed experiment.
6. Experimental Results – Clearly present all experimental data. Use tables to organize the values. Plots necessary graphs (should not be free hand). Label all tables, figures, equations appropriately.
7. Calculations – Show all calculations required to turn the measurement data into useful information and other require results.
8. Discussion and Conclusion – Perform a comparison of the theoretical results with actual results. Explain possible difference. Discuss any problems encountered and how they were resolved. Discuss the final results of the experiment and what insight was gained.
9. References – References used including textbook.
10. Appendices – Appendix should include the lab handout with the description of the experiment. Add other supporting materials if necessary.

Design

Several experiments will include logic circuits that must be designed by the student to meet the specifications that will be given at least one week in advance. The design (work and final circuit) will be due at the beginning of the lab.

Computer Usage

Several of the circuits shall be simulated and analyzed using Multisim.

Academic Integrity

Academic integrity is fundamental to the process of learning and evaluating academic performance. Academic dishonesty will not be tolerated. Academic dishonesty includes, but is not limited to, the following: cheating, plagiarism, tampering with academic records and examinations, falsifying identity, and being an accessory to acts of academic dishonesty.

Please refer to the UNO Student Policies for further information
http://www.uno.edu/studentaffairs/student-policies/.
The Academic Dishonesty Policy is available online at
http://www.uno.edu/studentaffairs/sa-documents/academicdishonestypolicy.pdf