Fall 12-20-2018

Performance Optimization of the Differential Protection Schemes

Monir Hossain
University of New Orleans, mhossai2@uno.edu

Performance Optimization of the Differential Protection Schemes

A Dissertation

Submitted to the Graduate Faculty of the
University of New Orleans
in partial fulfillment of the
requirements for the degree of

Doctor of Philosophy
in
Engineering and Applied Science
Electrical Engineering

by

Monir Hossain

B.S. Bangladesh University of Engineering and Technology, 2008
M.S. University of New Orleans, 2016

December, 2018

Acknowledgement

First, I would like to express my gratitute to my Ph.D. Supervisor, Dr. Ittiphong Leevongwat, who always encouraged my curiosity and kept me on the right track for the completion of this research. I would also like to extend my thanks to Dr. Parviz Rastgoufard, whose insight into the Power System world is nothing short of a blessing to me. I thank Dr. Linxiong Li, Dr. Leszek Malkiniski, and Dr. Ebrahim Amiri for taking the time to be a part of the dissertation committee.

I would like to thank my wife, parents, all close relatives and friends for their never ending support and encouragement, without whom I could not bear the struggle of a Ph.D. program. Lastly, I would like to thank the University of New Orleans for providing me with a quality education.

Contents

List of Figures

List of Tables

Abstract

Current differential protection principle is superior in terms of sensitivity and speed of operation in compare with other protection principle used in power systems. From last five decades, various current differential protection schemes are widely used to protect busbars, transformers and short-transmission lines. The deployment of high capacity microwave and optical fiber technologies redefined the line protection systems by facilitating the use of current differential protection schemes for long transmission lines. The common application issue of these schemes is mis-operation due to current transformer (CT) saturation during close-in external faults. Moreover, transformer differential protection schemes face mis-trip due to inrush current during energization. The techniques presented in the literature to address those issues, de-sensitize protection function and increase the time of operation. A comprehensive fault discrimination algorithm and an inrush current detection algorithm are highly demanded for current differential protection schemes. The purpose of this dissertation is to optimize the performance of differential schemes applied to protect busbar, transformer and line. This research derives the mathematical model of saturated secondary current of CT and introduces the concept of Partial Operating Current (POC). Based on these mathematical developments, the characteristics of POC are identified for all three types of differential zones like busbar, transformer and line protection. A new inrush current blocking algorithm is developed for transformer differential protection. A new time-domain CT saturation detection algorithm is also proposed. Based on these new development, three separate differential schemes are designed for busbar, transformer, and line protection, respectively. The proposed schemes provide complete immunity against the mis-operations due to CT saturation during close-in external faults and transformer inrush current without sacrificing the sensitivity for internal faults. The speed of operation is also improved. The model for each scheme is built in Matlab platform and the performance is validated using the test system simulated in Electro-Magnetic Transient Program (EMTP) for all possible

fault scenarios. Documented results show the improved performance of the proposed schemes when compared to traditional differential schemes in terms of reliability, sensitivity, selectivity and speed.

Key Words: Differential Protection, CT Saturation, Internal Fault, External Fault, Fault Discrimination, Inrush Current, Relay, Busbar, Transformer, Transmission Line.

Chapter 1

Introduction

Chapter 1 provides a general idea about a power system and its protection philosophy. Literature review of current differential protection is presented. The basic and historical review of the current transformer (CT) saturation and transformer inrush current are also described. Finally, the scopes of dissertation are presented.

1.1 Overview of Power Systems

Modern power systems are the combination of various complex elements such as generators, transformers, transmission lines, loads and protection and control equipments. Generally, power systems are divided into three stages: generation, transmission and distribution. The most convenient method to generate electricity is to burn fossil fuels to convert water into steam which is used to rotate a turbine that is connected to the rotor shaft of an electric generator. Water is also used to turn generators in hydro-electric power plant. In the last few decades, various new sources of electricity has been introduced which is called renewable energy such as solar, wind, geothermal and biomass etc. In all cases, the electricity generated at these facilities flows across the transmission system. Voltage at the generating stage is normally low, and hence, the generated voltage is raised by using step-up transformers to transmit power over long distance to reduce the higher voltage level transmission loss by reducing current. At the end of transmission system, voltage is stepped down by using step down transformer for power flow through distribution system and for supplying to residential and commercial customers.

The primary goal of any electric power utility is to provide uninterrupted power to the end consumer, and to achieve the goal, electric utilities depend on protection systems to provide protection to power systems equipment and elements such as generators, transformers, bus bars, overhead transmission lines operating in abnormal or fault conditions.

Most important criteria of power systems are the balance between generation and demand and to maintain the balance, utilities all over the world use various control systems such as supervisory control and data acquisition (SCADA) system and automatic generation control (AGC) system.

1.2 Overview of Power System Protection

The main purpose of a power system protection is to isolate a faulty section of the electrical power system from rest of the healthy systems so that the remaining live portion can function satisfactorily without any severe damage due to fault current [1]. Identification fault and isolating faulty part from the remaining healthy systems to secure the continuation of power supply are not straightforward.

The elementary power system protective device is the fuse. When the current through a fuse exceeds a certain threshold, the fuse element melts and produces an arc across the resulting gap that is then extinguished to interrupt the circuit [2]. Given that fuses can be built as the weak point of a system, fuses are ideal for protecting circuits from damage. Fuses however have two problems: first, after they have functioned, fuses must be replaced as they cannot be reset. This can prove inconvenient if the fuse is at a remote site or a spare fuse is not on hand. And second, fuses are typically inadequate as the protective device in most power systems as they allow current flows well in excess of that that would prove lethal to a human or animal. In general, fuses are used to protect simple and low power equipments. They are not suitable to use as the sole safety device in modern day high voltage and complex power systems.

Modern day's power system protection schemes are very sophisticated. They are built by integrating various complex devices or components. Circuit breaker, relay and DC system are the three main components of any protection scheme of power systems. All of these three components of protection scheme work simultaneously to give effective security against faults. Circuit breaker isolates the faulty system from rest of the healthy system and this

circuit breakers automatically open during fault condition due to its trip signal comes from protection relays [1].

Depending on arc quenching mechanisms, circuit breakers are classified as bulk oil circuit breaker, minimum oil circuit breaker, SF6 circuit breaker, air blast circuit breaker and vacuum circuit breaker etc. They are also classified as solenoid circuit breaker, spring circuit breaker, pneumatic circuit breaker, hydraulic circuit breaker etc. depending on operating mechanisms. Power system protection relays are classified as current relays, voltage relays, impedance relays, power relays, frequency relays, etc. based on operating parameter. As per operating characteristics, they are categorized as definite time relays, inverse time relays, stepped relays etc. According to operating logic, they are categorized as over current relays, distance relay and differential relays etc.

All the circuit breakers of electrical power systems are DC (Direct Current) operated. Because DC power can be stored in battery and if situation comes when total failure of AC power occurs, still the circuit breakers can be operated for restoring the situation by the power of storage battery . Hence the battery is another essential item of the power system protection. Some time it is referred as the heart of the electrical substation. An electrical substation battery or simply a station battery containing a number of cells accumulate energy during the period of availability of AC supply and discharge at the time when relays operate so that relevant circuit breaker is tripped.

The main philosophy of protection is that no protection of power systems can prevent the flow of fault current through the system, it only can prevent the continuation of flowing of fault current by quickly disconnect the short circuit path from the system [1, 3]. Protection systems should have several important functional requirements to satisfy this quick disconnection. Reliability is the most important requisite of power system protection. The protection relays should remain inoperative for a long time before a fault occurs; but if a fault occurs, they must respond instantly and correctly. Selectivity is another important requisite of power system protection schemes. Relays should be operated in only those fault

conditions for which schemes are commissioned in the system. There may be some typical condition during fault for which some relays should not be operated or operated after some definite time delay and so protection relays must be proficient to select appropriate condition for which it would be operated.The protective relays must be sufficiently sensitive so that it can be operated reliably when level of fault condition just crosses the predefined set limit. Another important requisite of protection systems is the speed of operation. The protective schemes must operate within set time duration after detecting fault. There must be a correct coordination provided in various power system protection relays in such a way that for the fault at one portion of the system should not disturb other healthy portions [4, 5]. Fault current may flow through a part of healthy portion as they are electrically connected. However, relays associated with that healthy portion should not be operated faster than the relays of faulty portion otherwise undesired interruption of healthy systems may occur. If relay associated with faulty portion is not operated in proper time due to any defect in it, then only the next relay associated with the healthy portion of the system must be operated to isolate the fault [4,5]. Therefore, it should neither be too slow which may result in damage to the equipment nor should it be too fast which may result in undesired operation

1.3 Literature Review of Current Differential Protection

Protection systems applied to protect the power system are classified into two categories - unit protection and non-unit protection. Differential protection is a unit protection system which is applied to protect a particular unit such as transformer, bus and transmission line. A unit is known as zone in protection terminology which is equivalent to a simple electrical node. A unit or zone is bounded by CT locations. There are mainly two types of differential protection based on the principles of operation - current balance differential protection and voltage balance differential protection. This paper investigates the current balance differential protection. As state in Kirchhoff's current law, the operating current which is defined by the vector summation of all CT secondary currents involved with protected zone is equal

to zero under normal operating condition. However, in fault conditions this vector sum is not equal to zero [6]. The operating current was used to drive the trip coil in conventional electro-mechanical differential relays in the past. Practically summation of the secondary current is not zero even for normal operating conditions, resulting in a false operating current due to the mismatching of CT characteristics, CT secondary cable impedance mismatch, and CT measuring errors. This false operating current is directly related to system loading or congestion. The concept of percentage restrained characteristics current has been introduced to overcome these issues [7]. There are several mathematical definitions of restrained current [8–10]. In most cases, the restrained current is defined by half of the summation of secondary current magnitudes of all CTs involved within a protected zone [10]. Under normal operation and external fault conditions, a relay remains inactive as the operating current is less than a percentage of restraining current. However, the operating current becomes greater than a percentage of restrained current during an internal fault and the relay operates .Two main application concerns reported with conventional current differential protection techniques which include mis-trip during close-in external faults due to CT saturation and mis-trip resulted from inrsuh current during transformer energization.

1.3.1 Bus Differential Protection

Several techniques were proposed based on CT saturation detection supervision to prevent mal operation of bus differential relay during CT saturation in external fault. However, they are failed to provide complete solution as CT can also be saturated during internal fault. A harmonic-current-based restraining method was introduced by Kennedy and Hayward [11]. If the harmonics contained in the differential current are larger than the threshold, the relay is inhibited. The method ensures stability on an external fault, but delays the operating time of a relay for an internal fault until after the DC component decays to a low value. When a CT saturates, the operating time is significantly increased. An algorithm that detects the onset of CT saturation based on the first-difference function of the current was described

by Phadke and Thorp [12]. It assumes the current immediately collapses to zero when the CT enters saturation. Difficulties arise if the current does not collapse to a low value during saturation. A solid-state busbar protection relay was proposed by Royle and Hill [13]. The relay detects the onset of saturation by detecting when the current collapses to a low value. It then shunts the current away from the operating circuit by closing a switch adjacent to the saturated CT. Although this technique prevents an external fault, the relay causes an operating time delay when a CT saturates on an internal fault. A microprocessor-based busbar protection relay that included a countermeasure for CT saturation was reported by Andow et al. [14]. The waveform discriminating element (WDE) is based on the assumption that the differential current during an external fault is nearly zero between the periods that corresponds to CT saturation. The WDE detects the onset of saturation by comparing the change in the instantaneous differential current against the instantaneous restraining current. The relay is inhibited for a predetermined period if the former is significantly less than the latter. The WDE is unable to indicate which CT is saturated and the blocking scheme may delay the operation of the relay on an internal fault. In addition, for a power system with a large primary time constant, a larger blocking period is needed and consequently a longer operating time delay is inevitable.

An impedance-based CT saturation detection algorithm for busbar differential protection was described by Fernandez [15]. The detection algorithm relies on the assumption that the current is decreased during saturation and thus the impedance is increased. The impedance is calculated at the relaying point and compared with the source impedance. If the estimated impedance is larger than the source impedance, saturation is detected and a blocking signal is issued. The algorithm is only valid if, after fault occurrence, the change in the impedance is negligible until saturation starts. Thus, it is difficult to detect saturation when the impedance increases significantly after fault occurrence. In addition, the algorithm uses a voltage signal to detect saturation and thus can cause an increase in the operating time. A microprocessor-based bus bar protection system that estimates the impedances of

the positive- and negative sequence circuits for every feeder connected to the busbar was proposed by Gill et al. [16]. The basic idea of the algorithm is similar to phase angle comparison. It compares the direction of current flow for each feeder and consequently is less dependent on the effect of CT saturation than a magnitude comparison algorithm [17]. The technique detects an internal fault if all the impedances seen by every feeder are located in the third quadrant of the impedance plane. The performance of the technique is satisfactory for mild saturation. However, correct operation of the technique is not guaranteed for severe saturation caused by a high level of remnant flux. Moreover, the technique requires significant computational burden as compared with phase angle comparison, since it calculates the positive- and negative sequence components of the voltages and currents for every feeder. Yong-Cheol Kang et al., has proposed a bus differential relay which operates in conjunction with a saturation detection algorithm based on the third-difference function applied to the current signal [18].

A wavelet transform (WT) based busbar protection scheme that utilizes detail decomposition of differential current to detect internal faults [19]. The algorithm relies on the assumption of time shift in transients between differential current and source current as most of the connected elements are inductive. However, the transients associated with the source current and the fault current are independent of location of fault (internal or external) which leads to mal-operation of the protection scheme. A backup protection is proposed based on polarities of peak d-coefficients obtained from Multi Resolution Analysis to prevent this mal-operation; even then, this technique is vulnerable at CT saturation and high impedance internal fault.

The preservation of current phase angle always takes place even if CT saturation or dc offset conditions occur to the input ac currents. As a result, if the phase angle of the current waveforms is compared with the phase angle of each of the input bus currents, a decision can be made whether a fault is external or internal to the differential protected zone irrespective of the waveform distortions due to the errors in CTs. Comparing phase currents

in near real time, a comparison can be made between currents that are entering the bus and those currents that are leaving the bus. This is intuitively true since Kirchoff's law also applies to phase angles as well as to current magnitudes. However, the key challenge in this method is estimation of phase angles between all current phase angles rapidly in real time. A technique based on dot product was used in reference [10, 20] to determine the differences in phase angles. This technique is suitable for transformer differential protection where two input currents are involved. But it is critical to implement for bus bar differential protection as more than two input currents are involved. Moreover, during a high impedance internal bus fault, load flow may continue to flow on passive elements and may cause the phase angles function to block the relay from tripping for the internal fault.

A fault discrimination method was proposed based on differential rate of change of operating current and restrained current [20]. The detection algorithm relies on the assumption that for an internal bus fault, the rate of change of operating current is greater than the rate of change of restrained current whereas for external faults, the rate of change of restrained current is greater than the rate of change of operating current. This technique provides security for low CT saturation during external fault. However, it has limitation for severe CT saturation as change of operating current becomes high as soon as CT starts saturated.

A different technique has been proposed based on alienation concept in order to determine busbar fault type whether internal or external to make relay trip or no trip decision, respectively [21–23]. The variance between any two signals is defined as the alienation coefficient, which is obtained from correlation coefficient. For internal fault, alienation coefficient is greater than zero and for external fault it is less than zero. In case of CT saturation, this technique compares the alienation coefficients of unsaturated portion and saturated portion of current to discriminate the fault. It assumes current remains unsaturated in first quarter cycle. This technique provides security for slow CT saturation during external fault. However, it leads mal-operation for severe CT saturation as CT starts saturated in first quarter cycle.

1.3.2 Transformer Differential Protection

Transformer is one of the most expensive assets of power systems; therefore, it is vital to have sensitive and reliable protection systems to protect transformers from faults. Any prolonged fault in transformer zone not only can result in severe damage to transformers but may end up being a cause of massive customer interruption. Therefore, accurate fault detection and quick clearance of faults are crucial for any transformer protection scheme. Differential protection has been the first choice of relay engineers for transformer protection since its invention. Differential protection has also been proved as one of the simplistic yet most reliable and efficient protection schemes for transformers. However, this relay may maloperate due to system disturbances, especially transformer inrush current and current-transformer (CT) saturation caused by an external fault.

To avoid maloperation due to the inrush current, it is common practice to utilize the ratio of the second harmonic component of the differential current to its fundamental harmonic component. In this approach, the differential relay should be blocked when the current ratio exceeds a predefined set value [24]. Although this approach is widely utilized in commercial relays, it may impose an extra time delay on the operation of a differential relay due to the following points: 1) for the cases where the fault current includes a decaying dc component, the defined current ratio may temporarily become more than the set value, which blocks the differential relay for one or two cycles; 2) when a transformer with an internal fault is energized, the differential relay may be blocked for even ten cycles [25]; 3) reliable estimation of the first and second harmonic components can lead to about one cycle of extra delay. The associated delay may result in more damage to healthy parts of the transformer which increases the required repair time and expense. In addition, the current harmonic approach cannot detect large inrush currents which occur after energizing a transformer with a considerable remanent flux, especially for newly designed transformers.

Another key challenge faced by transformer differential schemes is mis-trip resulted from current transformer (CT) saturation during close-in external faults. The reason for such mis-

operation is that the conventional differential principle focuses only on differential current magnitude for tripping decision which is inadequate in case of CT saturation. Therefore, proper discrimination of external and internal faults is the main hindrance to achieve the expected performance by transformer differential schemes. Several adaptive restraint differential characteristics techniques have been proposed to rectify the CT saturation issue since the invention of percentage restraint characteristic by McColl [26]. The restraint characteristics provide some security against CT errors for higher value of slope settings [7]; however, higher value of slope settings may reduce sensitivity for some in-zone faults [27]. A multi-region differential relay has been proposed by Hamed Dashti and Majid Sanaye-Pasand [24], where they have defined a control region in restraint-operational plane to declare external faults during CT saturation. However, some internal faults, especially the internal faults that evolve from external faults, can easily enter the defined control region and jeopardize the relay performance. An enhanced power transformer differential protection scheme has been presented in [28] based on the trajectory of the fault on restraint differential plane to improve security and dependability. The proposed scheme enhances the security when compared to traditional daul-slope percentage differential transformer protection; however, it delays the tripping speed during internal fault cases. Another adaptive transformer differential scheme has been introduced in [29] based on fault component calculated from recursive phasor estimation. The proposed scheme provides a certain degree of security against CT errors by sacrificing the degree of sensitivity for some in-zone faults.

Numerous trip blocking schemes have been proposed based on the supervision of various fault discrimination techniques to overcome the maloperation during external faults due to CT saturation. Harmonic-current-based blocking or restraining method [11] presented by Kennedy and Hayward ensures stability during external faults, but delays the operating time of a relay for an internal fault until after the DC component decays to a low value. Moreover, it may block internal faults in case of CT saturation. The scheme which includes fault discrimination method based on phase angle [10, 30] suffers from lack of sensitivity for

high impedance internal faults. A fault discrimination algorithm [31] was proposed relying on the assumption that for an internal fault, the rate of change of operating current is greater than the rate of change of restrained current. The method provides security for late CT saturation during external faults; however, it fails to secure blocking external faults in case of fast CT saturation. Recently researchers have explored new dimensions and proposed fault discrimination methods based on artificial neural network (ANN) [32–34], fuzzy logic [35–37], wavelet analysis [38–41], and empirical Fourier transform [42]to supervise a transformer differential scheme. However, the performance of these techniques depends on a large set of training data, or transformer parameters and initial conditions. Moreover, they increase compututional burden of the differential relay.

1.3.3 Line Differential Protection

Among power system elements, transmission lines are most vulnerable as they are distributed in wide geographical area and remained open in the air. Faults by means of short circuit can occur under a various environmental circumstances such as lightning, contact with trees and vegetations, contact with derbies carried by stormy wind or tornedo, insulator failure due to contamination, arc resistance and thunder storm. Therefore, transmission lines demand most sophisticated protection systems from the very beginning of power systems history.

Faults causes sudden and significant changes in the system quantities which includes current, voltage, phase angle, current direction, frequency, and impedance. Sudden and significant change in the line current is the most common fault indicator which leads to invention of over-current relays. Distance principle uses current and voltage information to calculate impedance and depending on the change of impedance, it distinguishes the faulty and normal conditions of power systems.

The protection philosopies mentioned above are categorized as single-ended system which are solely operated based on local end voltage and current information. The mesh nature of modern day power systems have fetched the challenge of co-ordination issue for all single

ended line portection systems which promotes the deployment of a newer technique, called pilot protection systems. Various types of pilot protection schemes were evolved over time incorporating different features to encounter the newer line protection challenges. Although, current differential protection principle is superior in terms of sensitivity and speed of operation as compared with other pilot protection schemes, it was not popular for line protection, sepecially for long line due to limitation of communication channel. However, the deployment of high capacity microwave and optical fiber technologies [43–45] redefined the line protection systems by facilitating the use of current differential protection schemes for long transmission lines.

Various line differential protection schemes [46–51] are reported in literature. Line current differential schemes work on either percentage restraint or alpha plane characteristics. CT saturation during close-in external fault is a primary challenge for both differential principles [52]. Various supervisory [49,53] and adaptive schemes [54–57] are introduced to address the security issues repoted for CT saturation; however, they desenitize the the phase differntial element. To re-gain the sensitivity, the application of zero-sequence and negative-sequence elements are encouraged in [49,58]. The application of zero-sequence and negative-sequence differential elements do not eliminate the necessity of phase differential element because sequence elements are unable to detect symmetrical internal faults. Moreover, both zero-sequence and negative-sequence differential elements have security concern for CT saturation events during external fault, single pole tripping and line impedance unbalance conditions [53, 58].

1.4 Current Transformer (CT) Saturation

Protective relays are actuated by current and voltage supplied by current and voltage transformers. These transformers provide insulation against the high voltage of the power circuit and also supply the relays with quantities proportional to those of the power circuit, but sufficiently reduced in magnitude so that the relays can be made relatively small and cost

effective. All types of current transformers are used for protective-relaying purposes. The bushing CT is almost invariably chosen for relaying in the higher-voltage circuits because it is less expensive than other types. It is not used in circuits below about 5 kV or in metal-clad equipment [3]. All CT accuracy considerations require knowledge of the CT burden. The external load applied to the secondary of a current transformer is called the burden. The burden is expressed preferably in terms of the impedance of the load and its resistance and reactance components. The term burden is applied not only to the total external load connected to the terminals of a current transformer but also to elements of that load.

Protective relay accuracy and performance are directly related to the steady state and transient performance of the CTs. Protective relays are designed to operate in a shorter time than the time period of the transient disturbance during a system fault. Large errors of CT transient may delay or prevent relay operation. CT output is impacted drastically when the CT operates in the nonlinear region of its excitation characteristic [59]. Operation in this region is initiated by:

- Large asymmetrical primary fault currents with a decaying dc component.
- Residual magnetism left in the core from an earlier asymmetrical fault, or field testing, if the CT has not been demagnetized properly.
- Large connected burden combined with high magnitudes of primary fault currents.

The instantaneous CT secondary current is the sum of the instantaneous burden current and the magnetizing current. The CT steady-state magnetizing current is very negligible as long as the CT operates in its linear region; therefore the burden current is a replica of the primary current adjusted by the CT ratio. When the CT is forced to operate in its nonlinear region, the magnetizing current can be very large due to a significant reduction of the saturable magnetizing inductance value. The magnetizing current which can be considered as an error current, subtracts from burden current and drastically affects the current seen by the connected burden on the CT secondary winding. When the CT saturates because of

the dc component, it can do so in the first few cycles of the fault. Long dc time constant offset faults can cause CTs to saturate many cycles after a fault [60].

Current differential protection is severely affected by the current transformer saturation during close-in external faults. This CT saturation creates high operating current in CT secondary circuit which causes the undesired operation of relay. Proper CT saturation detection is one of the major concerns to prevent mal-operation of bus bar differential protection.

A CT saturation algorithm has been proposed based on waveform model by A.G. Phadke and J. S. Throp [12]. It is based on the fact that secondary current is abruptly changed when CT saturation sets in. However, this algorithm fails when CT secondary current changes slowly. Another waveform method based on long data window has been proposed to detect CT saturation [61]. Computational time is comparatively high for this method because number of involved variables is more. Therefore, this method is slow to use together with any fast tripping algorithm. An algorithm based on the core flux calculating from a secondary current and then compensating the distorted secondary current was proposed [62]. The algorithm can successfully calculate the core flux and detect CT saturation in various conditions. However, this method is based on the assumption that the remanent (residual) flux at the beginning of calculation is zero.

Based on evaluating mean of error and the mean and variance of current amplitude, a CT saturation detection method was suggested [63]. The error is calculated on the assumption that the current is a perfect sinusoid. Hence the summation of the current and its second-order derivative should be zero. C. Fernandez has proposed an impedance-based CT saturation detection algorithm for bus-bar differential protection [15]. It is based on the first-order differential equation for the power system source impedance at the relay position and uses the busbar voltage as well as current signal to detect CT saturation.

An algorithm based on the third difference of a secondary current has been presented to CT saturation detection [64]. Third difference is more effective to detect CT saturation because it has large value than first and second difference. However, an anti-aliasing low-

pass filter softens the current and, thus, reduces the values of the third difference at those instants. Selection of sampling rate is very important to overcome the effect of a remanent (a term used by IEEE) flux in the core and a low-pass filter on the proposed algorithm.

A method based on symmetrical component analysis has been suggested to detect current transformer (CT) saturation [65].The proposed algorithm computes the positive-sequence negative-sequence and zero-sequence components of the differential current and also monitors the rate of change of the sequence component currents. The sequence component domain of differential current allows the differential protection scheme to more sensitively detect the system changing from a symmetrical condition to an asymmetrical fault condition. This concept is applied to detect CT saturation which gives an early indication of a CT being driven into saturation.

An algorithm has been developed to detect CT saturation by comparing the angle difference between the second harmonics of the rate of change of operating current and the rate of change of restrained current [66,67]. In this algorithm, the phase between the second harmonic of the derivatives of the operating current and restrain current is estimated and compared against the threshold value.

1.5 Transformer Inrush Current

Differential protection is considered the bestnprotection for transformers. However, inrush current due to transformer energization exists mostly only in one winding of the transformers; therefore, the differential relay sees the energization as a fault. To improve security while maintaining the required levels of deppendability, many methods using harmonic restraint, wave-shape recognition and artificial neural networks have been proposed to block the operation of the differential element due to the inrush current. The second harmonic restraint method is the most common one used by various relay manufacturers and application engineers [68]. The existence of a significant amount of escond harmonic component in the inrush current can be used to identify an energization event and to avoid false trip-

ping of differential protection. However, modern transformers may experience a very low level of second harmonic component in inrush current and may require an improved harmonic restraint method. In order to overcome the challenge of secure differential protection with low harmonic component in inrush current in new transformers, various harmonic restraint methods have been proposed [69–72] which include per-phase method, cross-blocking method, percent average blocking method and harmonic sharing method.

The above-mentioned methods may impose an extra time delay on the operation of a differential relay due to the following points: 1) for the cases where the fault current includes a decaying dc component, the defined current ratio may temporarily become more than the set value, which blocks the differential relay for one or two cycles; 2) when a transformer with an internal fault is energized, the differential relay may be blocked for even ten cycles [25]; 3) reliable estimation of the first and second harmonic components can lead to about one cycle of extra delay. The associated delay may result in more damage to healthy parts of the transformer which increases the required repair time and expense. In addition, the current harmonic approach cannot detect large inrush currents which occur after energizing a transformer with a considerable remanent flux, especially for newly designed transformers.

1.6 Scope of Dissertation

The purpose of this dissertation is to optimize the performance of differential schemes applied for busbar, transformer and line protection. This research derives the mathematical model of saturated secondary current of CT and a relation among Partial Operating Currents (POCs) and terminal currents. Partial Operating Currents (POCs) are found from successive vector addition of terminal currents. Based on these mathematical model, novel fault discrimination criterias are formulated for bus differential zone, line differential zone, and transformer differential zone. The new methods for CT saturation detection and inrush current blocking are proposed. Using these new developments, differential schemes are designed for busbar, transformer and line protection. Model for each scheme is built in Matlab platform and

the performance is validated using a transmission network simulated in Electro-Magnetic Transient Program (EMTP) for all possible fault scenarios. The proposed schemes provide enhanced immunity against the mis-operation due to CT saturation during close-in external faults without sacrificing the sensitivity for internal faults. The detail scope of works of the dissertation are shown in Figure 1.1.

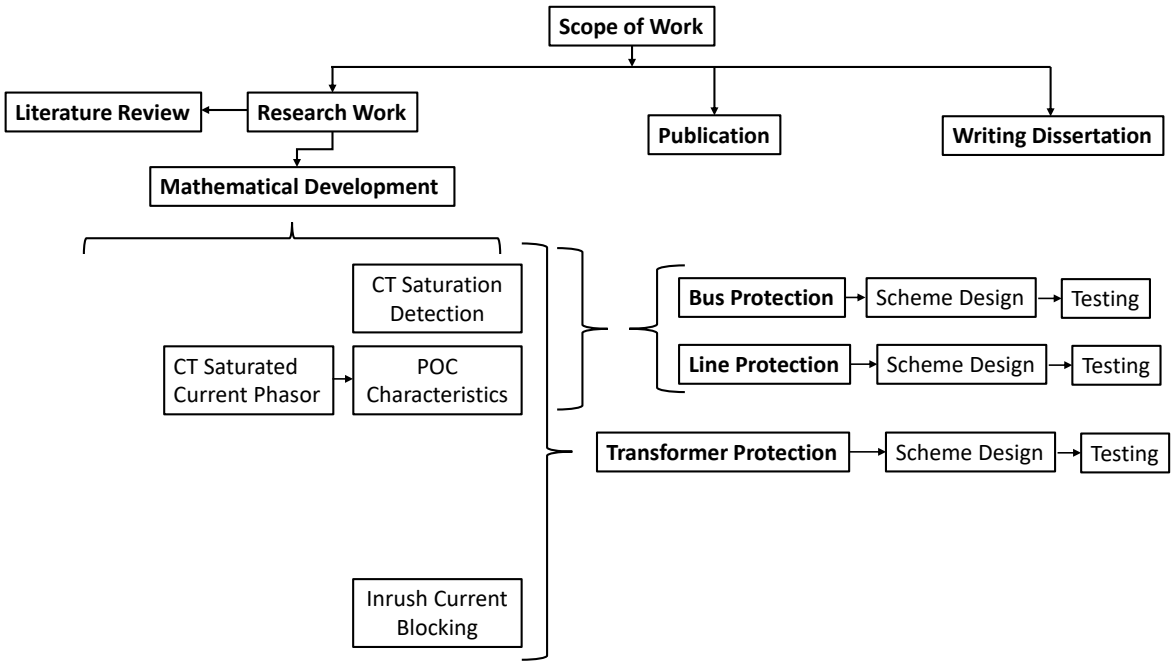

Figure 1.1: Scope of Works

Based on the research work, three journal (03) [74–76] and five (04) [77–80] conference papers have been published. Two (02) more journal papers [81, 82] are under preparation.

1.7 Summary

This chapter describes the background and literature review of differential protection schemes. The scope of works is also presented. The rest of the part of this dissertation is as follows. Chapter 2 describes the mathematical review. The problem formulation including mathematical development is presented in Chapter 3 based on [74, 76]. Chapter 4 describes proposed bus differential scheme based on [75]. Chapter 5 and 6 transformer and line differential

schemes based on [81] and [82], respectively.

Chapter 2

Mathematical Review

This chapter describes mathematical review of differential protection schemes used in power systems. The basic differential protection principles including the restraint characteristic and alpha plane characteristic are presented. The mathematical development of current transformer (CT) saturation is also discussed in detail. Finally, four existing fault discrimination algorithms are described.

2.1 Differential Protection Principle

Power systems can be divided into different blocks or units such as generator, transmission line, transformer, bus and motor etc. Protection schemes applied in the power system can be classified into two categories such as unit protection or non-unit protection. Current differential protection is the unit protection system which is applied to protect a particular unit. Unit is known as zone in protection terminology which is equivalent to simple electrical node. The unit or zone is bounded by CT locations.

2.1.1 Basic Differential Protection Principle

Kirchhoff's Current Law (KCL) is the principle of conservation of electric charge which implies that: at any node (Figure 2.1) in an electrical circuit, the sum of currents flowing into that node is equal to the sum of currents flowing out of that node, or equivalently the algebraic sum of currents in a network of conductors meeting at a point is zero [83].

Recalling that current is a signed (positive or negative) quantity reflecting direction towards or away from a node; this principle can be stated as Equation (2.1).

$$\sum_{i=1}^{n} I_n = 0 \tag{2.1}$$

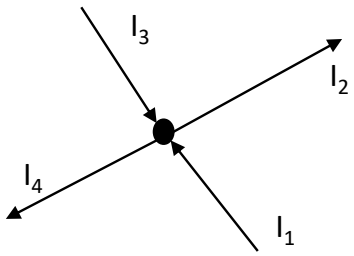

Figure 2.1: A typical electrical node

In Equation (2.1), n is the total number of branches with currents flowing towards or away from the node.

Kirchhoff's current law is based on the conservation of charge whereby the charge (measured in coulombs) is the product of the current (in amperes) and the time (in seconds). Differential protection works based on above mentioned Kirchhoff's current law. According to Kirchhoff's current law, under normal condition input current equals to output current for a power system zone [83]; therefore, vector summation of all terminal currents is zero. Practically summation of the currents is not zero even for normal operating conditions, resulting in a false operating current due to the mismatching of CT characteristics, CT secondary cable impedance mismatch, and CT measuring errors. This false operating current is directly related to system loading or congestion and can force the relay to mis-trip. To address the issue, the concept of percentage restrained and alpha plane characteristics have been introduced [7].

2.1.2 Restrained differential Protection

As mentioned earlier, the spill current resulted from the mismatching of CT characteristics, CT secondary cable impedance mismatch, and CT measuring errors, increases with the system loading; therefore, the flat differential over-current setting may result mis-trip during very high through current conditions (i.e. external faults). Considering these scenarios, researchers proposed various non-flat differential characteristics or slope differential

characteristics based on the relation between operating current (differential current) and restrained current. Here, the restrained current is the measure of system loading. Double slope restrained differential characteristic is shown in Figure 2.2 [7, 84].

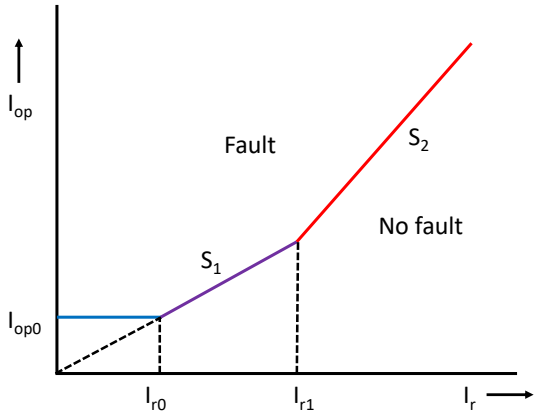

Figure 2.2: Characteristics curve of double slope restrained differential relay

The mathematical defination of operating current (I_{op}) is presented in Equation (2.2).

$$I_{op} = |I_1 + I_2 + ... + I_n| \tag{2.2}$$

There are several mathematical definitions of restrained current (I_r) as shown in Equations (2.3-2.5) [8–10].

$$I_r = |I_1| + |I_2| + ... + |I_n| \tag{2.3}$$

$$I_r = 0.5[|I_1| + |I_2| + ... + |I_n|] \tag{2.4}$$

$$I_r = max(|I_1|, |I_2|, ..., |I_n|) \tag{2.5}$$

In Equations (2.3)-(2.5): n is the number of terminals connected to the busbar and $I_1 - I_n$ represent corresponding terminal current phasors.

Depending on the value of I_r, the characteristic of percentage restraint fault detector shown in Figure 2.2 can be divided into three regions including $0 < I_r < I_{r0}$ (Region 1), $I_{ro} < I_r < I_{r1}$ (Region 2), and $I_r > I_{r1}$ (Region 3). The fault detection principle of each of the three regions is defined by Equations (2.6), (2.7), and (2.8), respectively.

Region 1:

$$I_{op} > I_{op0} \tag{2.6}$$

Region 2:

$$I_{op} > S_1(I_r - I_{r0}) + I_{op0} \tag{2.7}$$

Region 3:

$$I_{op} > S_2(I_r - I_{r1}) + S_1(I_{r1} - I_{r0}) + I_{op0} \tag{2.8}$$

In Equations (2.6)-(2.8): S_1 and S_2 are the first slope and second slope of the curve shown in Figure 2.2. The value of S_1 can vary from 0.1 to 0.7 [84]. The value of S_2 must be higher than S_1 can vary from 0.2 to 0.8 [84]. I_{op0}, I_{r0} and I_{r1} represent minimum operating current pickup, first transition point and second transition point respectively.

2.1.3 Ratio differential Protection

Ratio differential protection which is also known as Alpha plane used in zone differential protection is defined from the trajectory of the terminal current ratio (k) on the complex plane [46]. k is a complex number which is defined as the ratio of the phasor quantity of remote current (I_R) and local current current (I_L) as shown in Equation (2.9).

$$k = \frac{I_R}{I_L} \tag{2.9}$$

In alpha plane, two regions are identified as shown in Figure 2.3 including operating region for internal faults and blocking region for through-current conditions [46, 51, 58]. The typical values of radius R and angle α of the blocking region are 6 and 195° respectively, to

ensure security for external faults under CT saturation [85].

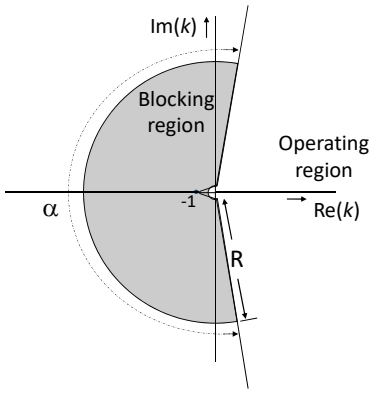

Figure 2.3: Characteristics curve of alpha plane

For multi-terminal application, Silva and et al introduced a generalized alpha plane concept in [51]. According to [51], for N terminals differential zone, operating current (I_{op}) and restraining current (I_r) are defined as shown in Equations (2.10-2.11).

$$I_{op} = \sum_{n=1}^{N} I_n = I_{op}^{re} + jI_{op}^{im} \tag{2.10}$$

$$I_r = \sum_{n=1}^{N} |I_n| \tag{2.11}$$

Aiming to apply the differential protection principle throughvthe alpha plane for the multiterminal equipment, it is necessary to map the N measured currents into two equivalent ones, here named as I_{op}^{eq} and I_r^{eq}. Therefore, the equivalent operating and restraining currents can be defined by Equations (2.12-2.13).

$$I_{op}^{eq} = I_{op} + I_r \tag{2.12}$$

$$I_r^{eq} = I_{op} - I_r \tag{2.13}$$

The equivalence between the actual and equivalent currents is guaranteed in case of the differential and restraining currents computed for both set of currents are equal. Thus, from Equations (2.10-2.13), one can obtain the following linear system of equations.

$$\begin{bmatrix} I_{op}^{re} \\ I_{op}^{im} \\ I_r \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \\ 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & -1 \end{bmatrix} \times \begin{bmatrix} I_{op}^{eq,re} \\ I_{op}^{eq,im} \\ I_r^{eq,re} \\ I_r^{eq,im} \end{bmatrix} \tag{2.14}$$

The solution of Equation (2.14) results Equations (2.15-2.16).

$$I_{op}^{eq} = 0.5[(I_{op}^{re} + I_r) + jI_{op}^{im}] \tag{2.15}$$

$$I_r^{eq} = 0.5[(I_{op}^{re} - I_r) + jI_{op}^{im}] \tag{2.16}$$

The ratio k is defined for muliterminal application by Equation (2.17).

$$k = \frac{I_{op}^{eq}}{I_r^{eq}} \tag{2.17}$$

2.2 CT Saturation

This section is written based on reference [86]. The circuit model of current transformer (CT) is shown in Figure 2.4.

The excitation characteristic of the CT is invariably a plot of secondary rms voltage versus secondary rms current, on log-log axes, as shown in Figure 2.5.

Two parameters S and VS can be extracted from the curve as shown in Figure 2.6.

The reason for choosing the saturation voltage, Vs, at the point where the excitation

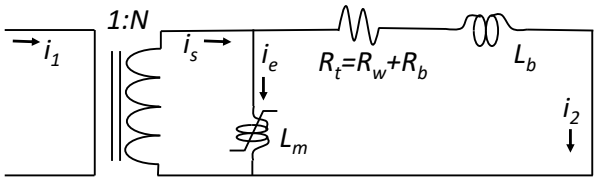

Figure 2.4: CT Circuit model

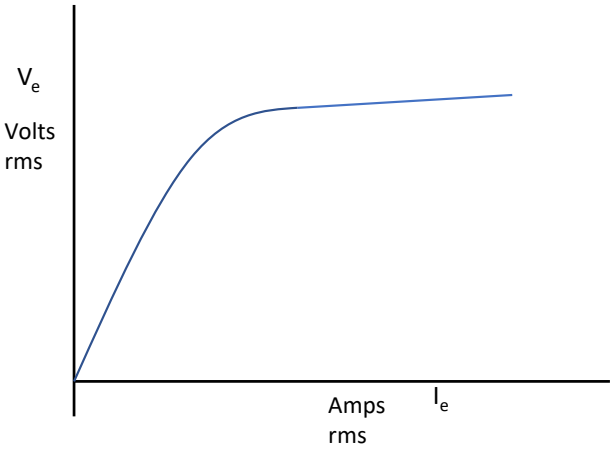

Figure 2.5: CT excitation curve, , redrawn from [86]

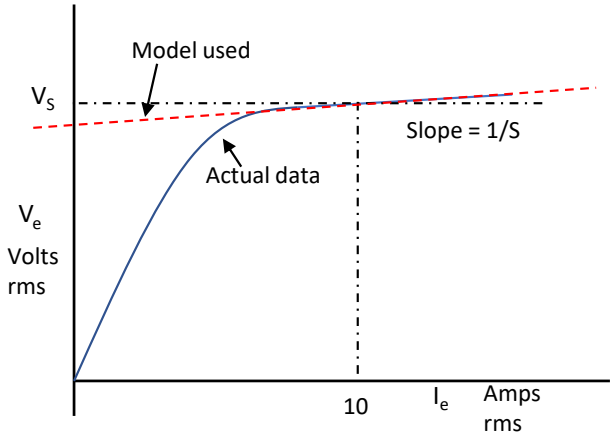

Figure 2.6: Method of determining the parameters Vs and S, redrawn from [86]

current is ten amps, is that this is the definition used in the standard [86]. The straight line curve with slope 1/S shown in Figure 2.6 is not linear. It is a curve defined mathematically as Equation (2.18).

$$logV_e = (1/S)logI_e + logV_i \tag{2.18}$$

In Equation (2.18), V_i is the value of V_e for I_e=1 , that is for $logI_e$=0. Equation (2.19) can be deduced by removing the logs from both sides of Equation (2.18).

$$V_e = V_i I_e^{1/S} \tag{2.19}$$

In order to solve the circuit of Figure 2.4, the instantaneous λ (flux-leakage) versus ie curve is required. It is postulated that a curve defined by Equation (2.20) is suitable as long as the exponent S is an odd integer [86].

$$i_e = A.\lambda^S \tag{2.20}$$

In order to allow S to be any positive number, and keep the function odd, the expression described in Equation (2.21), can be used.

$$i_e = A.sgn(\lambda).|\lambda|^S \tag{2.21}$$

In Equation (2.21), sgn(λ) is the sign of λ as shown in Figure 2.7 and A is a constant.

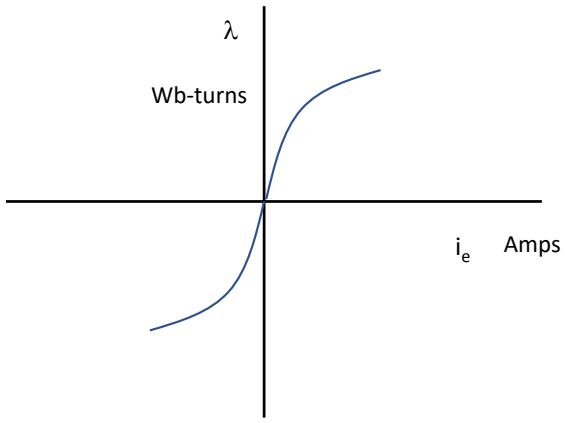

Figure 2.7: Postulated instantaneous values saturation curve, redrawn from [86]

The flux-linkage λ is related to the instantaneous excitation voltage V_e by Faraday's law [87] as Equation (2.22).

$$v_e = d\lambda/dt \tag{2.22}$$

The excitation voltage is assumed sinusoidal as Equation (2.23), which implies that the flux-linkage is also sinusoidal as Equation (2.24).

$$v_e = \sqrt{2}V_e \sin(\omega t) \tag{2.23}$$

$$\lambda = (1/\omega)\sqrt{2}V_e \sin(\omega t) \tag{2.24}$$

The resultant excitation current as shown in Equation (2.25) is non-sinusoidal, since it is a Sth order function of λ.

$$i_e = A.\lambda^S = A[(1/\omega)\sqrt{2}V_e]^S \sin^S(\omega t) \tag{2.25}$$

The rms value of i_e is given as Equation (2.26).

$$I_e = \sqrt{((1/2\pi)\int_0^{2\pi} i_e^2 dt)} \tag{2.26}$$

Equation (2.26) results the value of I_e as Equation (2.27).

$$I_e = A[\sqrt{2}V_e/\omega]^S \sqrt{(1/(2\pi)\int_0^{2\pi} \sin^{2S}(\omega t)dt)} \tag{2.27}$$

The ratio of rms-value-to-peak-value (RP) of the excitation current can be defined as Equation (2.28).

$$RP = \sqrt{(1/(2\pi)\int_0^{2\pi} (\sqrt{2}I_e)^2 \sin^{2S}(\omega t)dt)/\sqrt{2}I_e)} \tag{2.28}$$

Equation (2.28) can similified as Equation (2.29).

$$RP = \sqrt{(1/(2\pi)} \int_0^{2\pi} \sin^{2S}(\omega t) dt \tag{2.29}$$

The difference between RP for a sinusoid and RP the assumed excitation current waveform is illustrated in Figure 2.8. The factor RP gets smaller as the value of S increases.

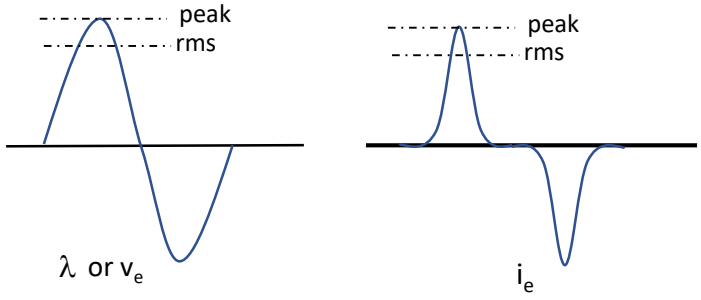

Figure 2.8: Comparison of the rms/peak relationship for two wave shapes, redrawn from [86]

Equation (2.30) is deduced from Equations (2.27) and (2.29).

$$I_e = A[\sqrt{2}V_e/\omega]^S RP \tag{2.30}$$

By substituting the value of $V_e = V_S$ at I_e=10 (as shown in Figure 2.6) in Equation (2.30), the value of A can be deduced as Equation (2.31).

$$A = 10\omega^S/(\sqrt{2}V_S.RP) \tag{2.31}$$

Equation (2.32) is derived from Equations (2.30) and (2.31).

$$i_e = sgn(\lambda).|\lambda|^{1/S}.10\omega^S/(\sqrt{2}V_S.RP) \tag{2.32}$$

Now, applying Kirchhoff's Voltage Law around the right-hand loop of the circuit in Figure 2.4, yields Equation (2.33).

$$v_e - (i_s - i_e)R_t - L_b.d/dt(i_s - i_e) = 0 \tag{2.33}$$

The solution of i_s is given in Equation (2.34).

$$i_s = \sqrt{2}I_p/N[Off.e^{-t/\tau} - \cos(\omega t - \cos^{-1} Off)] \tag{2.34}$$

In Equation (2.34), Off = per unit dc-offset magnitude and τ = system time constant. The derivative of i_s is given in Equation (2.35) [84].

$$di_s/dt = \sqrt{2}I_p/N[-Off/\tau.e^{-t/\tau} + 1/\omega.\cos(\omega t - \cos^{-1} Off)] \tag{2.35}$$

Equation (2.36) is deduced from Equation (2.20).

$$di_e/dt = di_e/\lambda.d\lambda/dt = A.S.|\lambda|^{S-1}.d\lambda/dt \tag{2.36}$$

Using Equations (2.22) and (2.36), Equation (2.33) can be re-written as Equation (2.37).

$$d\lambda/dt[1 + L_b.A.S.|\lambda|^{S-1}] = -i_s.R_t + i_e.R_t + L_b.di_s/dt \tag{2.37}$$

The above first-order nonlinear differential equation is solved for $\lambda(t)$ using standard numerical analysis techniques. Using the resultant $\lambda(t)$, i_e is calculated by Equation (2.20). Then the actual secondary current i_2 is calculated as Equation (2.38).

$$i_2 = i_s - i_e \tag{2.38}$$

In case of the single-valued saturation curve, conventional remanence is not possible because non-zero λ cannot occur for zero ie . However, remanence can be approximated very closely by simply assuming that the initial excitation current is non-zero. For convenience, λ_{rem} is expressed in per unit of V_S as Equation (2.39) (Figure 2.9).

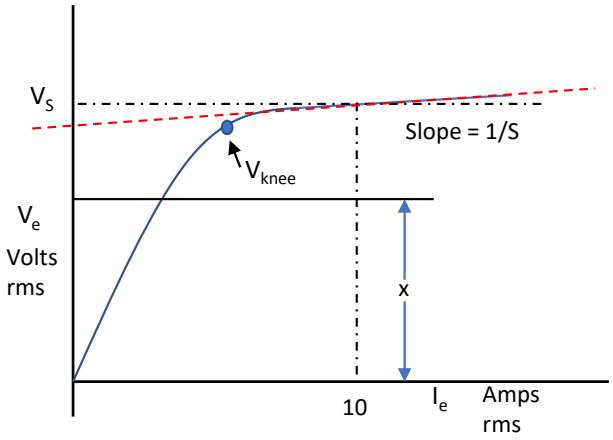

Figure 2.9: Definition of per unit remanence, redrawn from [86]

$$\lambda_{rem} = x/V_S \tag{2.39}$$

In order to specify λ_{rem} accurately, x must be specified not greater than V_{knee} [86].

2.3 Transformer Inrush Current

Transformer experiences magnetizing inrush current during energization. Inrush current occurs in a transformer whenever the residual flux does not match the instantaneous value of the steady-state flux which would normally be required for the particular point on the voltage waveform at which the circuit is closed [88, 89].

For the explanation of the mechanism causing inrush current in a transformer's primary winding when connected to an AC voltage source, Equation (2.40) is considered, where and λ and v are the instantaneous flux in a transformer core and voltage drop across the primary winding, respectively.

$$v = \frac{d\lambda}{dt} \tag{2.40}$$

According to the Equation (2.40), the rate of change of instantaneous flux in a transformer core is proportional to the instantaneous voltage drop in the primary winding or on the other

hand, the flux waveform is the integral of the voltage waveform. In continuously-operating transformer, these two waveforms are shifted by 90°. But a significant difference exists between continuous-mode operation and energization of a transformer. During continuous operation, the flux level is at its negative peak when voltage is at its zero point, but during energization the flux has to start at zero [68]. So, for a rising voltage just started from zero, the magnetic flux will reach approximately twice its normal peak as it integrates the area under the voltage waveform's first half-cycle. This amount of flux, because of the nonlinear characteristic of the magnetization curve, causes saturation of the transformer. During saturation, disproportionate amounts of mmf are needed to generate magnetic flux. This means the winding current, which creates the mmf to cause flux in the core, will disproportionately rise to a value easily exceeding twice its normal peak [88].

According to [88], the general equation that gives the amplitude of inrush current as a function of time can be expressed as Equation (2.41).

$$i(t) = \frac{\sqrt{2}}{Z_t} \times V_m \times K_w \times K_s \times (sin(\omega t - \phi) - \exp[\frac{-(t - t_0)}{\tau}] \times sin\alpha) \tag{2.41}$$

In Equation (2.41), V_m is maximum applied voltage, Z_t is total impedance under inrush, ϕ is energization angle, t is time, t_0 is point at which core saturates, τ is time constant of transformer winding under inrush conditions, α is function of t_0, K_w is accounts for 3 phase winding connection, and K_s is accounts for short-circuit power of network [88].

Inrush current $i(t)$ can be expressed as Equation (2.42) in terms of harmonic components.

$$i(t) = I_0 + \sum_{h=1}^{\infty} a_h \cos(h\omega t) + b_h \sin(h\omega t) \tag{2.42}$$

In Equation (2.42), I_0 is DC offset and h represents harmonic number. The constants a_h and b_h are described in Equations (2.43) and (2.44).

$$a_h = \frac{1}{\pi}\int_0^{2\pi} i_{sat}(t)cos(h\omega t)d\omega t \tag{2.43}$$

$$b_h = \frac{1}{\pi}\int_0^{2\pi} i_{sat}(t)sin(h\omega t)d\omega t \tag{2.44}$$

2.4 Existing Fault Discriminating Algorithms

2.4.1 Phase Angle Comparison Algorithm (PACA)

Phase angle comparison algorithm was proposed in [10, 20, 90] to overcome the issue of CT saturtion. Phase angle comparison principle monitors the phase angle relationships of the incoming and the outgoing currents of a protected zone. Phase angle differences among various incoming and outgoing currents are determined in real-time using the dot product method. If phase angle differences are within a threshold value, the zone of protection is considered being under an internal fault. If the threshold is exceeded, the zone is under an external fault. For any two current phasors I_{pi} and I_{pj}, the dot product can be expressed by Equation (2.45), where "p" represents phase A, B, or C.

$$I_{pi}.I_{pj} = |I_{pi}||I_{pj}|cos\theta_{ij} \tag{2.45}$$

Equation (2.45) can be re-written as Equation (2.46).

$$cos\theta_{ij} = (I_{pi}.I_{pj})/(|I_{pi}||I_{pj}|) \tag{2.46}$$

The term $cos\theta_{ij}$ directly indicates the phase difference between the two currents. For an n-terminal protected zone where $i, j = 1, 2, ..., n$ and $i \neq j$, if $cos\theta_{ij}$ is greater than a specific threshold value $cos\theta_0$ for all combinations of i and j, then the metric of Equation (2.47) indicates existence of an internal fault.

$$I_{pi}.I_{pj} > |I_{pi}||I_{pj}|cos\theta_0 \tag{2.47}$$

According to the definition of internal faults [10, 20, 90], $\theta_0 = 90°$; however, typically θ_0 is set to $75° - 85°$ in practice. During a high-impedance internal fault, small outbound currents through passive elements connected to a zone may invalidate the phase angle metric of Equation (2.47) resulting in a block of relay tripping. Therefore, a setting parameter I_{th} is used to check each terminal phasor current. Any phasor current with a magnitude less than the set value of I_{th} is excluded from the PACA algorithm. Typically, I_{th} is set to the value of charging current of the longest transmission line connected to the bus (zone).

2.4.2 Rate of Change of Differential Algorithm (ROCODA)

Rate of change of differential algorithm proposed in [20, 90] uses rate of change of operating and restraint current to discriminate the differential currents resulted from internal faults and CT saturation during external faults. For an n-terminal protected zone, operating current I_{op} and restraint current I_r are defined by Equations (2.48) and (2.49).

$$I_{op} = |I_{p1} + I_{p2} + ... + I_{pn}| \tag{2.48}$$

$$I_r = 0.5(|I_{p1}| + |I_{p2}| + ... + |I_{pn}|) \tag{2.49}$$

ROCODA algorithm [20, 90] declares a fault as an internal fault if the fault satisfies two conditions. First, the rate of change of operating current dI_{op}/dt as well as the rate of change of restraint current dI_r/dt must be positive. To verify the first condition, the rate of change of operating current dI_{op}/dt as well as the rate of change of restraint current dI_r/dt are compared with a small positive threshold value I_0. Secondly, dI_{op}/dt must be greater than dI_r/dt. The output of ROCODA is a logic high when the two conditions are satisfied. Once the output becomes high due to an internal fault, it remains at high state as long as the fault exists.

2.4.3 Alienation Coefficient Algorithm (ACA)

Alienation coefficient algorithm was proposed in [21–23] to address the CT saturation issue of bus differential protection during external faults. The variance between any two signals is defined as the alienation coefficient [21, 50] which is the indicator of non-similarity between two signals. Alienation coefficient calculated between two current signals found from the two-terminal equivalent representation of a multi-terminal differential zone for each phase, is used to determine the fault type whether internal or external to make relay trip or no trip decision, respectively [21–23]. The two-terminal equivalent representation of a multi-terminal differential zone is obtained by dividing all terminal currents of each phase into two groups and then adding the currents of each group. The resultant equivalent currents of two groups are represented by i_{pE1} and i_{pE2} respectively. Correlation coefficient (r_p) between the two equivalent currents i_{pE1} and i_{pE2} is calculated by Equation (2.50).

$$\begin{aligned} r_p = (\sum_{l=1}^{m} i_{pE1}(l) i_{pE2}(l) - (1/m) \sum_{l=1}^{m} i_{pE1}(l) \sum_{l=1}^{m} i_{pE2}(l))/ \\ \sqrt{((\sum_{l=1}^{m} (i_{pE1}(l))^2 - (1/m)(\sum_{l=1}^{m} i_{pE1}(l))^2)(\sum_{l=1}^{m} (i_{pE2}(l))^2} \\ -(1/m)(\sum_{l=1}^{m} i_{pE2}(l))^2)) \end{aligned} \tag{2.50}$$

In Equation (2.50), m represents sample size per cycle. The alienation coefficient Ap is defined by Equation (2.51).

$$A_p = 1 - (r_p)^2 \tag{2.51}$$

It is known that during normal operation or external faults without CT saturation, i_{pE1} is equal to i_{pE2}; therefore, A_p is zero. During internal faults, the alienation coefficient between i_{pE1} and i_{pE2} becomes high instantaneously after fault inception [21–23]. During external

faults with CT saturation, the alienation coefficient between i_{pE1} and i_{pE2} remains very low (close to zero) during the first one-eighth (1/8) cycle after fault inception [21–23], and then becomes high. A small positive value A_x is used in ACA to compare with A_p. If alienation coefficient rises above A_x during the first one-eighth (1/8) cycle after fault inception, then the fault is an internal fault; otherwise the fault is detected as an external fault. Once the output of ACA becomes high due to an internal fault, high state continues during the existence of the fault.

2.4.4 Second Harmonic Blocking Method

The second harmonic blocking tecnique is used to improve the security of transformer differential protection against the inrush current due to transformer energization. Inrush current contains different harmonic components. Horowitz shows in [91] that second harmonic component is the most prominent one in transformer inrush current. This is why researcher proposed a transformer differential blocking or restraint method based on the ratio of second harmonic component to the fundamental component. Transformer differential protection is blocked when the ratio of second harmonic component to the fundamental component is greater than a set value. The typical value of the threhold is 0.171 [89,92]. According to [68], the mathematical development of the second harmonic blocking method is presented below.

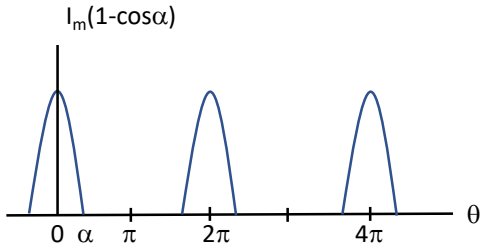

Figure 2.10: Idealized inrush current waveform, redrawn from [68]

The simplified wave shape of the typical inrush current is shown in Figure 2.10. The idealized inrush current shown in Figure 2.10 can be presented mathematically as Equation (2.52), where l =[-∞, ∞].

$$i_{sat}(t) = \begin{cases} I_m(cos\theta - cos\alpha), & (2l\pi) < \theta < (2l\pi + \alpha) \\ I_m(cos\theta - cos\alpha), & (2l\pi - \alpha) < \theta < 2l\pi \\ 0, & otherwise \end{cases} \tag{2.52}$$

Based on Fourier analysis, the peak fundamental component is given by Equation (2.53).

$$a_1 = \frac{I_m}{\pi}[\alpha - 0.5 \times sin(2\alpha)] \tag{2.53}$$

The second harmonicl component is given by Equation (2.54).

$$a_2 = \frac{I_m}{\pi}[-0.167 \times sin(3\alpha) + 0.5 \times sin(\alpha)] \tag{2.54}$$

The ratio of second harmonic component to the fundamental component is given by Equation (2.55).

$$\frac{a_2}{a_1} = \frac{-0.167 \times sin(3\alpha) + 0.5 \times sin(\alpha)}{\alpha - 0.5 \times sin(2\alpha)} \tag{2.55}$$

According to [68], $\alpha = \frac{2\pi}{3}$ when residual flux is 90 percent and saturation flux is 140 percent of the rated peak flux. Equation (2.55) results in the ratio equals to 0.171 when $\alpha = \frac{2\pi}{3}$.

2.4.5 Summary

This chapter has covered the mathematical development of current differential protection which includes restraint and alpha plane characteristics. Mathematical modeling of CT saturation as well as transformer inrush current have been described. Mathematical background

of four widely used fault discrimination algorithms have also been presented in details.

Chapter 3

Problem Formulation: Mathematical Development

This chapter starts by describing the problem statement and objective of the dissertation. The research workflow is described in steps. Finally, the contributed mathematical developments are presented which include, modeling of CT saturated phasor quantity [76], analytical model of Partial Operating Current (POC) [73,74], mathematcal model of a waveform-based inrush current blocking algorithm, and mathematical model of a CT saturation detection algorithm are presented based on [78–80]. POC is used to develop an algorithm which discriminate between internal faults and CT saturation during external faults. The proposed inrush current detection algorithm enhances security of transformer differential protection; however, reduces tripping time in case of a transformer energization with interal fault. The proposed CT saturation detection algorithm is used to supervise the differential protection logic to enhance sensitivity against current inversion scenarios which may occur due to high fault impedance or having series capacitor in line.

3.1 Problem Statement: Difficulties in Discriminating Faults

Recently, micro-processor based current differential protection schemes have become popular to protect busbar systems, transformers and transmission line. Current differential protection schemes are operated based on operating current which is the summation of all CT secondary currents. Practically summation of the secondary current is not zero even for normal operating conditions as accurate matching of characteristics of current transformer cannot be achieved hence there may be spill current flowing through the relay in normal operating conditions. Moreover, there may be a probability of mismatching in cable impedance from CT secondary to the remote relay panel. These uneven pilot cables' capacitance causes high current through the relay operation coil when large external through fault occurs. This operating current is known as false operating current and it becomes high during high load-

ing conditions or high system congestion. To overcome these issues, the concept of restrained current characteristic and alpha plane characteristic have been adapted with current differential schemes.

The main application issue with this restrained differential protection is to make it secure from mal-operation in response to the CT saturation during close-in external faults. During close-in external faults, probability of CT saturation becomes high and this CT saturation creates high operating current in CT secondary circuit which causes the undesired operation of relay. The primary reason for such mal-operation is the fact that the traditional percentage differential principle relies exclusively on current magnitude rather than directionality for tripping decisions.

There are several existing techniques to discriminate between internal fault and external fault for bus differential protection. CT saturation detection supervision is one of the earliest techniques, however, it fails to provide complete solution as CT can also be saturated during internal fault. Phase Angle Comparison Algorithm (PACA) is very widely used technique, although it has computational complexity when large numbers of input currents are involved. Moreover, during a high impedance internal bus fault, load flow may continue to flow on passive elements which may cause the phase angles function to block the relay from tripping for the internal fault. The Rate of Change of Differential Algorithm (ROCODA) works based on rate of change of operating and restrained current which has limitation on fast CT saturation condition. Traditional Alienation Coefficient Algorithm (ACA) requires instantaneous fault detection to trigger the timer which is quite challenging in practical application.

Various alpha plane characteristics are used in line differential protection to address the security issues repoted for CT saturation; however, they desenitize the the phase differntial element. To re-gain the sensitivity, the application of zero-sequence and negative-sequence elements are encouraged in [49, 58]. The application of zero-sequence and negative-sequence differential elements do not eliminate the necessity of phase differential element because sequence elements are unable to detect symmetrical internal faults. Moreover, both zero-

sequence and negative-sequence differential elements have security concern for CT saturation events during external fault, single pole tripping and line impedance unbalance conditions [53, 58]. Another major application challenge of alpha plane characteristics is to detect internal faults which result in current inversion. Internal faults in series-compensated line can cause current inversion and the trajectory of the current ratio can be plotted inside the blocking region of alpha plane.

Therefore, proper discrimination method of external and internal faults for bubar, transformer, and transmission line is the demand of the modern power systems.

3.2 Objective

The purpose of this dissertation is to optimize the performance of differential schemes applied to protect busbar, transformer and line. This research derives the mathematical model of saturated secondary current of CT and introduces the concept of Partial Operating Current (POC). Based on these mathematical developments, the characteristics of POC are identified for all three types of differential zones like busbar, transformer and line protection. A new inrush current blocking algorithm is also developed for transformer differential protection. A new CT saturation detection algorithm is also proposed. Based on these new development, three separate differential schemes are designed for busbar, transformer, and line protection, respectively. The proposed schemes provide complete immunity against the mis-operations due to CT saturation during close-in external faults and transformer inrush current without sacrificing the sensitivity for internal faults. The speed of operation is also improved. The performances of each scheme are validated using the test system simulated in Electro-Magnetic Transient Program (EMTP) for all possible fault scenarios. Documented results show the improved performance of the proposed schemes when compared to traditional differential schemes in terms of reliability, sensitivity, selectivity and speed.

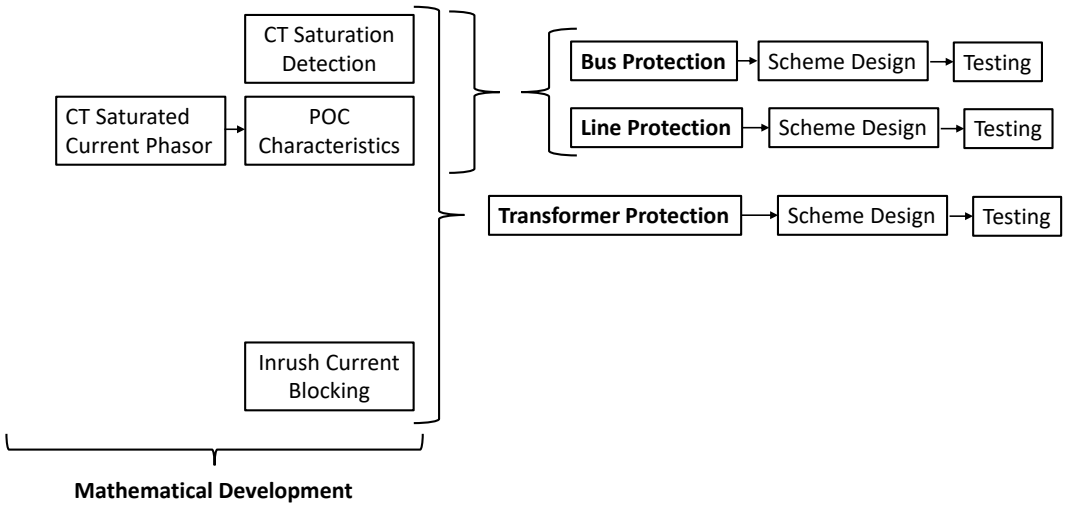

Figure 3.1: Research workflow diagram

3.3 Research Workflow

This section describes the workflow of this research work. As CT saturation is the common concern for all differential protection schemes respective of the application, this research work starts by exploring CT saturated current phasor characteristics. Based on the characteristics of CT saturated current phasor, the concept of Partial Operating Current (POC) characteristic is introduced. An analytical model of a time-domain CT saturation detection method is developed. This new CT saturation detection method and POC characteristic are used to discriminate the external and internal fault. The characteristics of the transformer inrush current waveform are explored to develop an inrush current blocking algorithm. This new inrush current blocking algorithm is used to supervise the transformer differential protection trip equation. Finally, three differential protection schemes are proposed for bus, transformer, and line protection. Three test systems are developed in EMTP for three applications respectiively. The performances of each scheme are validated using the test system simulated in Electro-Magnetic Transient Program (EMTP) for all possible fault scenarios.

Figure 3.1 shows the block diagram of the research work which has following steps.

1. Developing mathematcal model of CT saturation which describes the beheviors of current phasor with the change of CT saturation severity.
2. Developing analytical model of POC characteristics for the multi-terminal differential protection zone using mathematcal model of CT saturation.
3. Developing analytical model of CT saturation detection method.
4. Developing analytical model of inrush current blocking method based on current waveform.
5. Design bus differential protection scheme and testing the performance of the scheme.
6. Design transformer differential protection scheme and testing the performance of the scheme.
7. Design line differential protection scheme and testing the performance of the scheme.

3.3.1 Mathematical Model of CT Saturation

According to [86], the CT secondary current is calculated by the Equations (3.1-3.5) described below.

$$i_2 = i_s - i_e \tag{3.1}$$

$$i_s = i_p/N \tag{3.2}$$

$$i_e = A.\lambda^S = A[(1/\omega)\sqrt{2}V_e]^S \sin^S(\omega t) \tag{3.3}$$

$$\lambda(t) = \lambda(t-1) + d\lambda(t-1) \tag{3.4}$$

$$d\lambda/dt[1 + L_b.A.S.|\lambda|^{S-1}] = -i_s.R_t + i_e.R_t + L_b.di_s/dt \tag{3.5}$$

Equation (3.5) ia the first-order nonlinear differential equation which can be solved for $\lambda(t)$ using standard numerical analysis techniques. In this work, MATLAB function ODE45 is used to solve for $\lambda(t)$ and corresponding waveform of i_2 is shown in Figure 3.2.

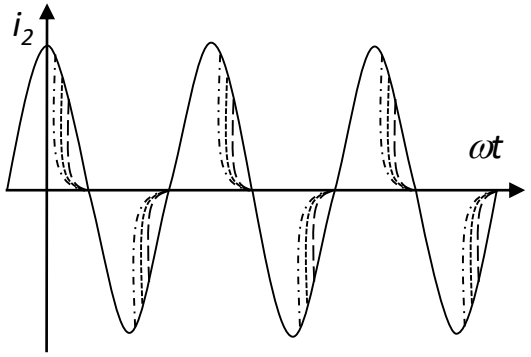

Figure 3.2: Waveform of i_2 (CT secondary current) for various saturation severity

From the waveform of saturated CT secondary current, the following three assumptions can be made.

1. CT secondary current becomes instantaneously zero when CT starts saturation.

2. It remains zero till the starting of 2nd half cycle.

3. CT saturation is periodic.

Considering above three assumptions,generalized saturated CT secondary current can be represented as shown in Figure 3.3, where θ represents distorted portion of the waveshape.θ also means the degree of saturation severity.

The generalized saturated CT secondary current can be represented mathematically by Equation (3.6).

$$i_{sat}(t) = Isin(\omega t), \qquad for\ 0 < \omega t < \pi - \theta\ and\ \pi < \omega t < 2\pi - \theta \tag{3.6}$$

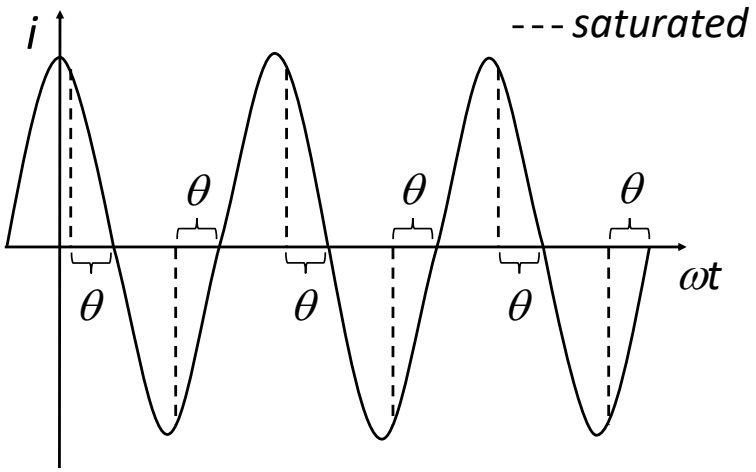

Figure 3.3: Generalized waveform of saturated CT secondary current

According to Fourier series, $i_{sat}(t)$ can be expressed as Equation (3.7).

$$i_{sat}(t) = I_0 + \sum_{h=1}^{\infty}(a_h cos(h\omega t) + b_h sin(h\omega t)) \tag{3.7}$$

In Equation (3.7), I_0 is DC offset and h represents harmonic number. The constants a_h and b_h are described in Equation (3.8-3.9).

$$a_h = (1/\pi)\int_0^{2\pi} i(t)cos(h\omega t)d\omega t \tag{3.8}$$

$$b_h = (1/\pi)\int_0^{2\pi} i(t)sin(h\omega t)d\omega t \tag{3.9}$$

For h-th harmonic component, phasor can be represented as Equation (4.10).

$$I_h = |I_h|\exp(j\phi_h) \tag{3.10}$$

In Equation (4.10), I_h and Φ_h are the h-th harmonic component magnitude and phase which can be found by Equation (3.11-3.12).

$$|I_h| = \sqrt{(a_h^2 + b_h^2)}/2 \tag{3.11}$$

$$tan(\phi_h) = -b_h/a_h \tag{3.12}$$

Instantaneous h-th harmonic current can be expressed as Equation (3.13).

$$i_h = |I_h| sin(h\omega t - \phi_h) \tag{3.13}$$

For fundamental component (h=1), a_1 and b_1 can be expressed in terms of θ as Equation (3.14-3.15).

$$a_1 = (|I|/2\pi)(1 - cos2\theta) \tag{3.14}$$

$$b_1 = (|I|/\pi)(\pi - \theta + 0.5sin2\theta) \tag{3.15}$$

Substituting the value of a_1 and b_1 in Equation (3.11-3.12), the magnitude and phase of fundamental component can be expressed as Equation (3.16-3.17).

$$|I_1| = (I/\pi\sqrt{2})\sqrt{(}0.5 - 0.125cos2\theta + (\pi - \theta)^2 + (\pi - \theta)sin2\theta) \tag{3.16}$$

$$tan(\phi_1) = 2(\pi - \theta + 0.5sin2\theta)/(cos2\theta - 1) \tag{3.17}$$

Figure 3.4 and 3.5 show the change of magnitude and phase of fundamental component with change of saturation severity (θ).

Figure 4.6 shows the trajectory of fundamental component in complex plane with change of saturation severity (θ).

3.3.2 Analytical Model of Partial Operating Current (POC) Characteristics

In power system, there are two types of differential protection zones: two-terminal such as transformers or transmission lines, and multiterminal zones such as busbars or multi-terminal lines. Figure 3.7 shows a typical multiterminal protection zone which has n terminals. Terminal is a branch-circuit where transmission line or generator or load is connected. The

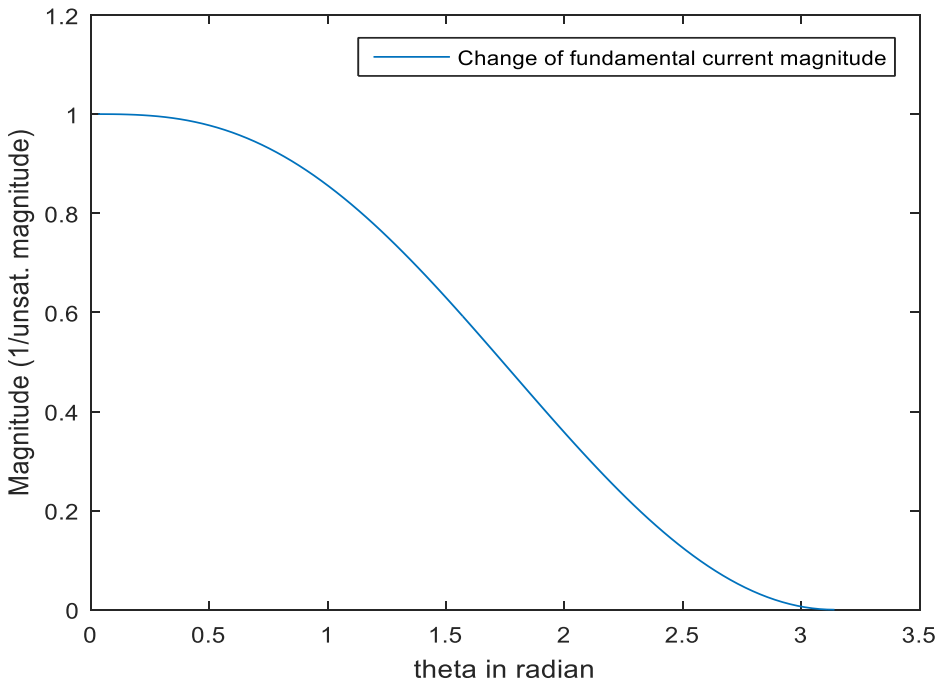

Figure 3.4: Change of magnitude with change of saturation severity (θ)

Fig.1 is the single phase representation of a three phase system. Based on Figure 3.7, an analytical model of partial operating current (POC) characteristics is derived below.

For n-terminal differential zone as shown in Figure 3.7, differential operating current is defined as Equation (3.18).

$$I_{op} = \sum_{j=1}^{n} I_j \tag{3.18}$$

In Equation (3.18) : n is integer, $n > 1$, and I_j corresponds to phasor current of each terminal shown in Figure 3.7. One key point needs to be mentioned that a phase shift can be occurred between input and output current phasors of transformer differential zone due to different winding connections. Therefore, all terminal currents need to be compensated by using appropriate compensation factor before applying any differential protection schemes

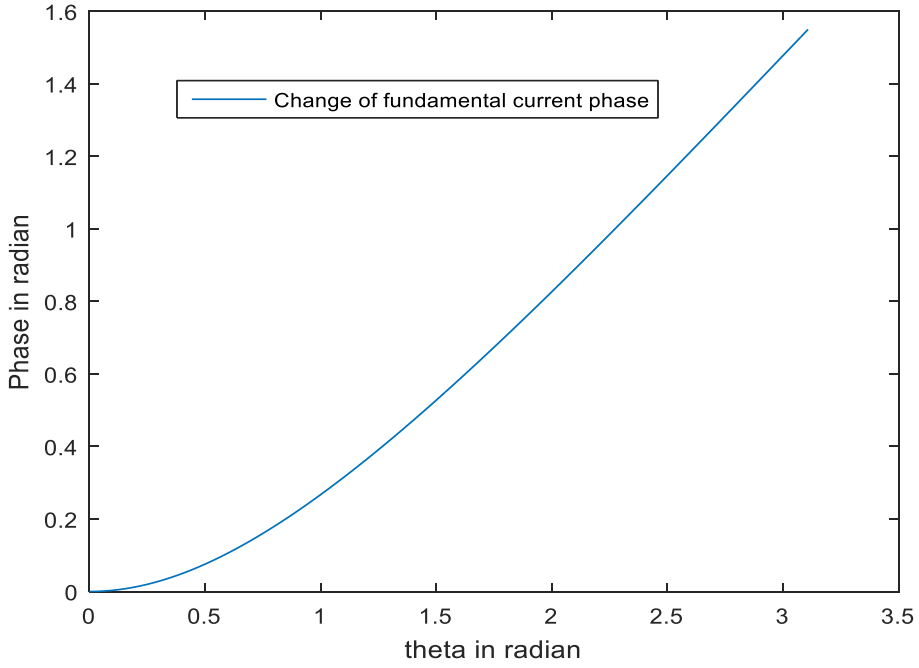

Figure 3.5: Change of phase with change of saturation severity (θ)

to protect transformer.

This paper presents the concept of new quantities called "Partial Operating Currents (POCs)" by successive addition of terminal currents as Equation (3.19).

$$I_{op(k)} = \sum_{j=1}^{k} I_j + I_{k+1} \tag{3.19}$$

In Equation (3.19), $I_{op(k)}$ represents k^{th} POC, where $k = 1, 2, ..., (n-1)$. Note that in an n-terminal zone, there are $(n-1)$ POCs. The final POC which is denoted by $I_{op(n-1)}$, is defined by Equation (3.20) and it is equal to the term differential operating current I_{op} appearing in Equation (3.18).

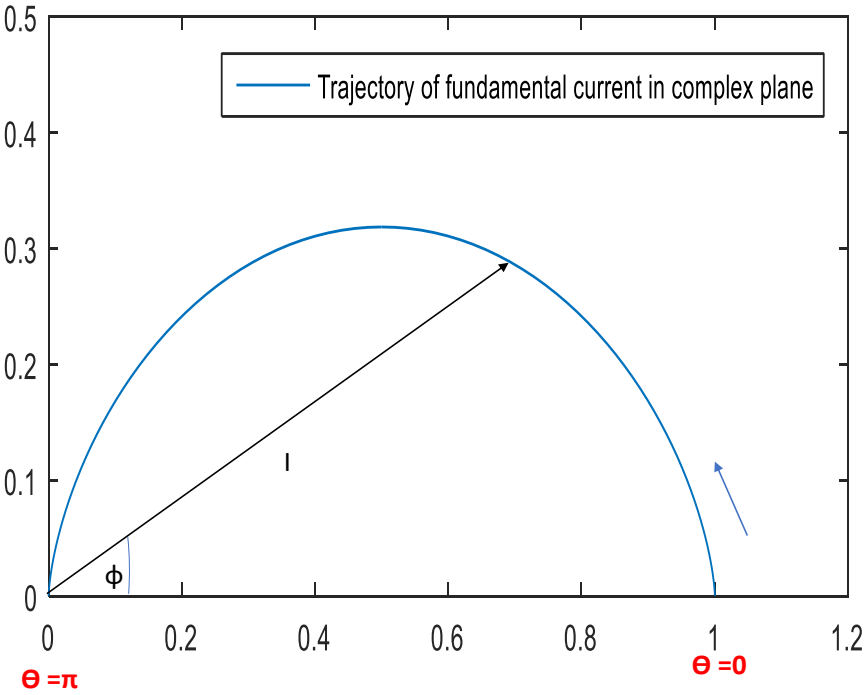

Figure 3.6: Trajectory of fundamental component in complex plane

$$I_{op(n-1)} = \sum_{j=1}^{n-1} I_j + I_n = \sum_{j=1}^{n} I_j = I_{op} \tag{3.20}$$

Based on Equation (3.19), the relation between two consecutive POCs can be expressed by recursive formula of Equation (3.21).

$$I_{op(k)} = I_{op(k-1)} + I_{k+1} \tag{3.21}$$

In Equation (3.21), $I_{op(k-1)}$ and I_{k+1} are defined as the input currents of resultant $I_{op(k)}$ with initial condition $I_{op(0)} = I_1$. Note that Equation (3.21) is true for both normal and faulted conditions which are described in subsequent sub-sections.

The operation of power systems is categorized as normal conditions or fault conditions. Faults can be categorized further as internal faults to the protection zone and external faults

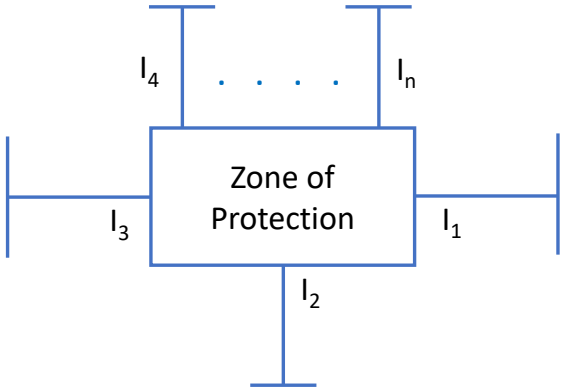

Figure 3.7: n-terminal differential zone

to the protection zone. The characteristic metrics of defined POCs corresponding to the three operation categories are described next.

3.3.2.1 Normal operation

Consider n-terminal differential protection zone as Figure 3.7 under normal operating condition where all n terminal current magnitudes are larger than zero. The direction of at least one terminal current must be opposite to other terminal currents to make the vector summation equal to zero ($I_{op} = 0$) according to KCL [83]; therefore, $I_{op(n-1)}$ appears as Equation (3.22).

$$I_{op(n-1)} = \sum_{j=1}^{n-1} I_j + I_n = I_{op} = 0 \tag{3.22}$$

Equation (3.23) can be deduced from Equation (3.24).

$$I_{op(n-2)} = \sum_{j=1}^{n-2} I_j + I_{n-1} = \sum_{j=1}^{n-1} I_j = -I_n \tag{3.23}$$

From Equation (3.24), $|I_{op(n-2)}|$ can be expressed as Equation (3.25).

$$|I_{op(n-2)}| = |I_n| \tag{3.24}$$

Using Equation (3.25)

$$max(|I_{op(n-2)}|, |I_n|) = max(|I_n|, |I_n|) = |I_n| > 0 \tag{3.25}$$

Based on Equation (3.21), $I_{op(n-1)}$ can be defined by Equation (3.26).

$$I_{op(n-1)} = I_{op(n-2)} + I_n \tag{3.26}$$

From Equations (3.22) and (3.25), the relation among resultant POC $I_{op(n-1)}$ and its two input currents $I_{op(n-2)}$, and I_n of Equation (3.26) could be described by Equation (3.27).

$$|I_{op(n-1)}| < max(|I_{op(n-2)}|, |I_n|) \tag{3.27}$$

Equation (3.27) indicates that there must be at least one resultant POC whose magnitude is smaller than the larger one of its two input currents under normal operation of a differential protection zone with any number of terminals.

3.3.2.2 Internal Fault

To derive the characteristics of POCs during internal fault conditions, we use properties of vector addition which are presented below.

Let's assume two non-zero vector quantities A and B and the angle between them represented by θ as shown in Figure 3.8. The vector C represents the resultant vector and its magnitude is expressed in terms of $|A|$, $|B|$, and θ as Equation (3.28).

$$|C| = (|A|^2 + |B|^2 + 2|A||B|cos\theta)^{1/2} \tag{3.28}$$

In the range of $\theta = 0° - 90°$, the maximum and minimum value of $|C|$ can be found at $\theta = 0°$ and $\theta = 90°$ respectively as expressed by Equations (3.29) and (3.30).

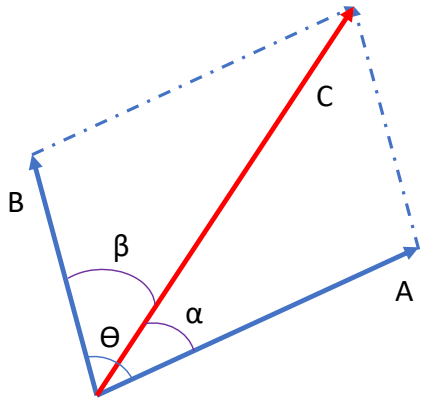

Figure 3.8: Vector addition

$$|C|^{max} = |A| + |B| \tag{3.29}$$

$$|C|^{min} = (|A|^2 + |B|^2)^{1/2} \tag{3.30}$$

From Equations (3.29) and (3.30), it can be deduced that $|C| > |A|$ as well as $|C| > |B|$ for the range of $\theta = 0° - 90°$ and this relation is described by Equation (3.31).

$$|C| > max(|A|, |B|) \tag{3.31}$$

The angle between A and C is α. The angle between B and C is β. Both α and β must be smaller than θ as Equation (3.32).

$$\alpha, \beta < \theta \tag{3.32}$$

Now, consider an internal fault at n-terminal differential zone shown in Figure 3.7. If there is any fault within the zone, currents from all terminals connected to the protection zone flow towards the zone [17,93], which indicates that all terminal currents during internal fault is literally in same phase given that the system is synchronized. In exception, a CT saturation during internal fault can create large phase angle difference between saturated

terminal current and other unsaturated terminal currents. Because when a CT saturates, the secondary current magnitude decreases and its angle advances [30]. However, when angle distortion approaches 90°, current magnitude approaches zero [58], which means possible maximum angle between any two terminal currents would be less than 90° in case of internal fault irrespective of CT saturation. In addition, a small current may continue to flow through passive elements connected to the zone during high impedance internal faults. The security against these scenarios can be increased by setting a threshold (I_0) to check each terminal current. If any terminal current is less than I_0, it would be excluded from POC calculation. I_0 would be set higher than the charging current of longest line connected to the zone or higher than the maximum possible load current connected to the zone [52].

Using Equation (3.32), it can be deduced that the resultant $I_{op(k)}$ from Equation (3.21), is in same direction with its two input currents $I_{op(k-1)}$, and I_{k+1} during internal fault for $k = 1, 2, ..., (n-1)$ because, possible maximum angle between any two POC's input currents is less than 90 degrees. Therefore, based on Equation (3.31), the relation among $I_{op(k)}$ and its two input currents $I_{op(k-1)}$, and I_{k+1} can be expressed as Equation (3.33).

$$|I_{op(k)}| > max(|I_{op(k-1)}|, |I_{k+1}|) \tag{3.33}$$

In Equation (3.33): k=1, 2, ..., (n-1) with intitial condition $I_{op(0)} = I_1$. Equation (3.33) states that each resultant POC is greater than the larger one of its two input currents for any n-terminal differential protection zone (where $n > 1$) for the case of internal fault conditions.

3.3.2.3 External Fault

During an external fault, current flows outbound from the protection zone through the faulted terminal [93,94], which means direction of the faulted terminal current is opposite to the other terminal currents. Normally, $I_{op} = 0$ for external fault conditions; however, I_{op} can be high due to CT saturation because when a CT saturates, the fundamental component

of the secondary current decreases in magnitude and its angle advances [30]. If CT is not saturated during external faults (no differential operating current exists), then POCs follow same characteristics as normal operational condition described in Sub-section 3.3.2.1.

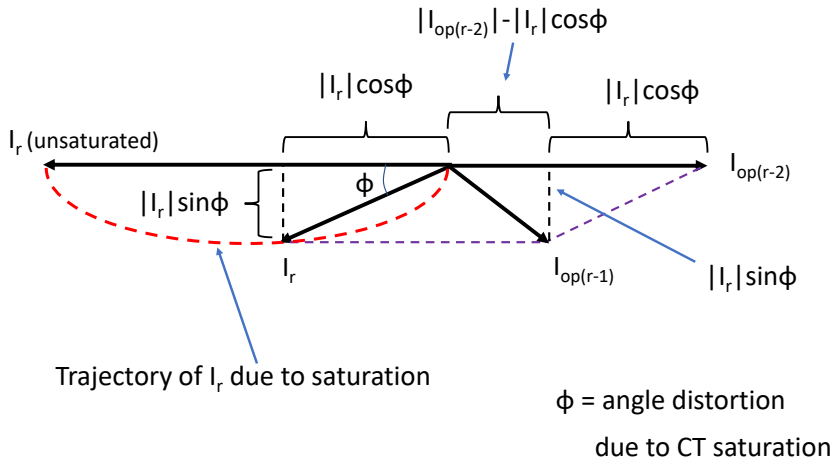

Figure 3.9: Trajectory of current phasor I_r due to CT saturation and corresponding resultant of vector addition

Now, assume that an external fault is incepted at terminal r (where $1 \leq r \leq n$) of n-terminal differential protection zone shown in Figure 3.7 and CT of terminal r is saturated. CT saturation results distortion in the magnitude of I_r (current of terminal r) and its phase angle; therefore, a differential current is in exist. In this case, $I_{op(r-2)}$ can be expressed by Equation (3.34).

$$I_{op(r-2)} = \sum_{j=1}^{r-2} I_j + I_{r-1} \tag{3.34}$$

Based on Equation (3.21),

$$I_{op(r-1)} = I_{op(r-2)} + I_r \tag{3.35}$$

The trajectory of current phasor described in Section 3.3.2 depending on CT saturation

severity is shown in Figure 3.9 for I_r. When angle distortion of I_r due to CT saturation approaches 90°, magnitude drastically approaches zero. From Figure 3.9, $|I_{op(r-1)}|$ can be expressed in terms of $|I_r|$, $|I_{op(r-2)}|$ and Φ as Equation (3.36).

$$|I_{op(r-1)}| = ((|I_{op(r-2)}| - |I_r|cos\Phi)^2 + (|I_r|sin\Phi)^2)^{1/2} \tag{3.36}$$

According to Section 3.3.2, $|I_r|$ and Φ can be expressed in terms of saturation severity (θ) as Equation (3.37-3.38).

$$|I_r| = (I_{unsat}/\pi\sqrt{2})\sqrt{(}0.5 - 0.125cos2\theta + (\pi - \theta)^2 + (\pi - \theta)sin2\theta) \tag{3.37}$$

$$tan(\phi) = 2(\pi - \theta + 0.5sin2\theta)/(cos2\theta - 1) \tag{3.38}$$

Practically, current never becomes completely distorted due to CT saturation, it remains undistorted in the first one-eighth (1/8) of each cycle [21] which means the value of θ can be varied in the range of 0 to $3\pi/4$. For $\theta = 0 - 3\pi/4$, it can be proved from Equation (3.36-3.38) that practical CT saturation hold Equation (3.39) true.

$$|I_{op(r-1)}| < max(|I_{op(r-2)}|, |I_r|) \tag{3.39}$$

Equation (3.39) indicates that at least one of the resultant POCs is smaller than the larger one of its two input currents for any differential protection zone during an external fault irrespective of CT saturation.

The above mathematical development shows that POCs have unique characteristics during internal fault conditions which are expressed in Equation (3.33). Equation (3.33) is a novel mathematical function to determine whether the directions of all terminal currents are the same or not, which eliminates the computational burden of angle measurement.

3.3.3 CT Saturation Detection

CT saturation can be detected using the time difference between fault inception and inception of CT saturation. CT does not start saturated at the instant of fault inception. According to [95,96], current waveforms remain undistorted at least for about 1/6 cycle before the first saturated waveform portion. The fast fault inception detection technique is proposed in [79] to determine fault inception time and alienation coefficient of equivalent two current signals is used to calculate the CT saturation starting time [80]. Mathematical development of fast fault detection method and alienation coefficient calculation are discussed below.

3.3.3.1 Fast Fault Inception Detection

The steady-state instantaneous current of k-th terminal (i_{pk}) connected to the differential zone can be expressed as Equation (3.40).

$$i_{pk}(t) = \sqrt{2} I_{pkm} \cos(\omega t + \theta_k) \tag{3.40}$$

In Equation (3.40): I_{pkm} is rms value of the current, ω is angular frequency and θ_k is phase shift.

The absolute value of first-derivative of $i_{pk}(t)$ is found as Equation (3.41).

$$\left|\frac{di_{pk}(t)}{dt}\right| = \sqrt{2}\omega I_{pkm} |\sin(\omega t + \theta_k)| \tag{3.41}$$

Equation (3.42) can be derived from Equation (3.41) since $|\sin(\omega t + \theta_k)|_{max}$ =1.

$$\left|\frac{di_{pk}(t)}{dt}\right|_{max} = \sqrt{2}\omega I_{pkm} \tag{3.42}$$

In steady-state rms value remains constant over time which means $I_{pkm}(t) = I_{pkm}(t-T)$,

where T = time period. Therefore, Equation (3.42) can be re-written as Equation (3.43).

$$|\frac{di_{pk}(t)}{dt}|_{max} = \sqrt{2}\omega I_{pkm}(t-T) \tag{3.43}$$

However, with the inception of any transient condition (i.e. fault), $i_{pk}(t)$ changes abruptly which results a huge value of $|\frac{di_{pk}(t)}{dt}|$ and the relation of Equation (3.44).

$$|\frac{di_{pk}(t)}{dt}| >> \sqrt{2}\omega I_{pkm}(t-T) \tag{3.44}$$

The Equation (3.44) can be equated as in Equation (3.45).

$$|\frac{di_{pk}(t)}{dt}| > S\sqrt{2}\omega I_{pkm}(t-T) \tag{3.45}$$

In Equation (3.45), S is a marginal constant to avoid mis-detection of fault inception in case of the change in terminal current during normal operating condition (i.e. load change). The value of S must be greater than 1 but not very large. The large value of S can affect the sensitivity of fault detector.

3.3.3.2 Alienation Coefficient

CT saturation distorts the current signal and alienation coefficient indicates the distortion of any signal. Therefore, alienation coefficient can be used to find the CT saturation starting time. The alienation coefficient (A_p) between two current signals is calculated from cross-correlation coefficient (r_p) as shown in Equation (3.46), where p = A, B or C phase.

$$A_p = 1 - (r_p)^2 \tag{3.46}$$

Cross-correlation coefficient (r_p) of two currents i_{pE1} and i_{pE2} is calculated by Equation (3.47) [21]. i_{pE1} and i_{pE2} are two equivalent currents found from the two-terminal equivalent

representation of a differential zone.

$$r_p = (\sum_{n=1}^{m} i_{pE1} i_{pE2} - (1/m) \sum_{n=1}^{m} i_{pE1} \sum_{n=1}^{m} i_{pE2})/ \sqrt{((\sum_{n=1}^{m} i_{pE1}^2 - (1/m)(\sum_{n=1}^{m} i_{pE1})^2)(\sum_{n=1}^{m} i_{pE2}^2 - (1/m)(\sum_{n=1}^{m} i_{pE2})^2))} \quad (3.47)$$

In Equation (3.47), m represents sample size per cycle. The two-terminal equivalent representation of a differential zone is obtained by using Dynamic Current Allocation Algorithm (DCAA) [78]. DCAA arranges all terminal currents of each phase into two groups, resulting in two equivalent currents i_{pE1} and i_{pE2}.

3.3.4 Inrush Current Blocking

Inrush current occurs in a transformer whenever the residual flux does not match the instantaneous value of the steady-state flux which would normally be required for the particular point on the voltage waveform at which the circuit is closed [68, 89, 92].Inrush current drawn by transformer during energization is typically asymmetrical as shown in Figure 3.10 [97] where, T and τ represent time period and base time, respectively. The base time (τ) is the time portion in one cycle period where current is non-zero.

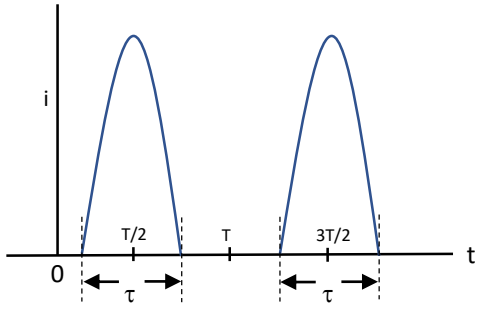

Figure 3.10: Typical inrush current waveform

For a transformer, the base time of inrush current depends on three factors which include residual flux, saturation flux and energization voltage angle. The base time of inrush current decreases as the energization voltage angle increases [68]. To find the maximum base time scenario, it is considered that the transformer energization starts at zero voltage angle as shown in Figure 3.11.

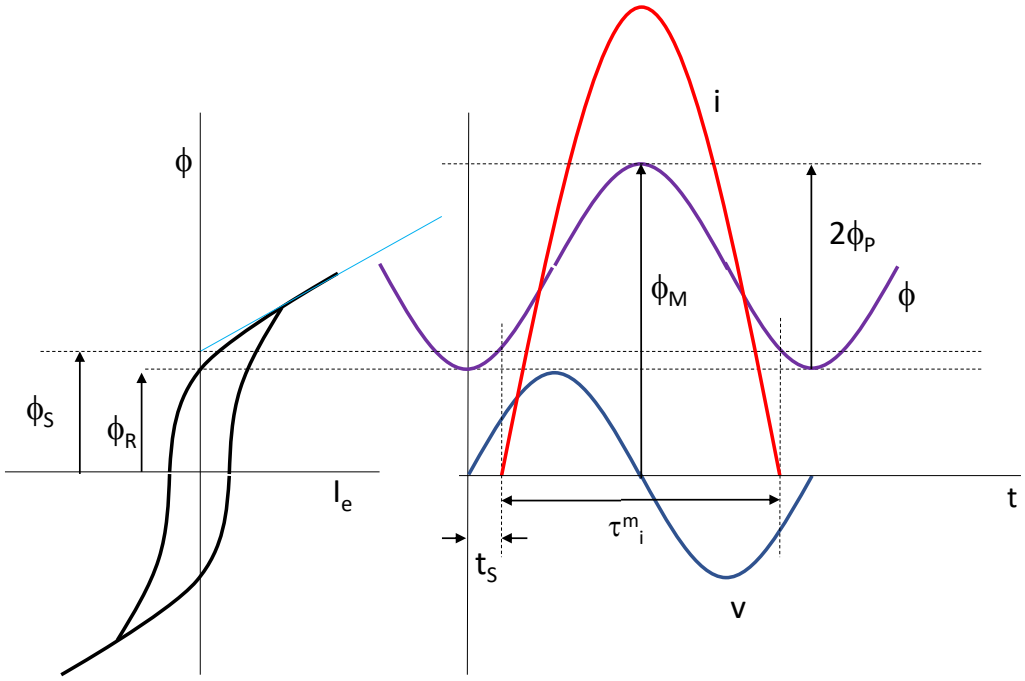

Figure 3.11: Excitation curve when transformer starts energization at sero voltage angle

Figure 3.11 shows maximum base time (τ_i^m) of inrush current is a function of residual flux (ϕ_R), saturation flux (ϕ_S), and rated flux (ϕ_P). Based on [68], the inrush current starts to flow at the instant when the transformer core flux hits the saturation flux and the instantaneous flux can be expressed as Equation (3.48).

$$\phi(t) = (\phi_R + \phi_P) - \phi_P cos(\omega t) \tag{3.48}$$

Equation (3.48) can be re-written as Equation (3.49) to find the value of t_S.

$$t_S = \frac{cos^{-1}(\frac{\phi_R+\phi_P-\phi_S}{\phi_P})}{\omega} \tag{3.49}$$

The maximum base time (τ_i^m) of the inrush current can be expressed as Equation (3.50).

$$\tau_i^m = (T - 2t_S) = (T - 2\frac{cos^{-1}(\frac{\phi_R + \phi_P - \phi_S}{\phi_P})}{\omega}) \tag{3.50}$$

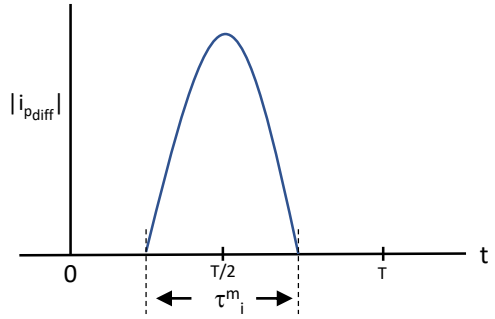

Figure 3.12: Differential current resulted from inrush current

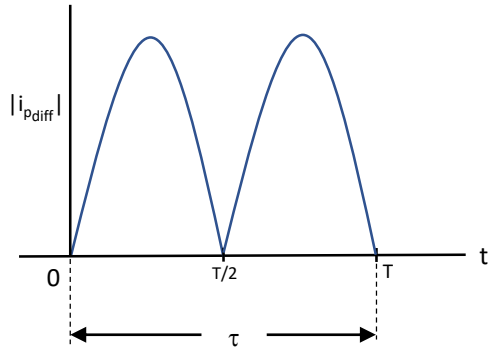

Figure 3.13: Differential current resulted from internal faults

The absolute value of instantaneous phase differential current ($i_{p_{diff}}$) is same as inrush current (p means phase), which shown in Figure 3.12 and corresponding base time (τ_i^m) is far less than one cycle [97]. The base time of $|i_{p_{diff}}|$ resulted from internal faults is ideally one cycle as shown in Figure 3.13. The above development defines the following conditions.

1. Inrush current events: $\tau \leq \tau_i^m$.

2. Internal fault events: $\tau > \tau_i^m$.

Based on above defined conditions, this research proposes an inrush blocking scheme.

3.3.4.1 Base time (τ) Calculation

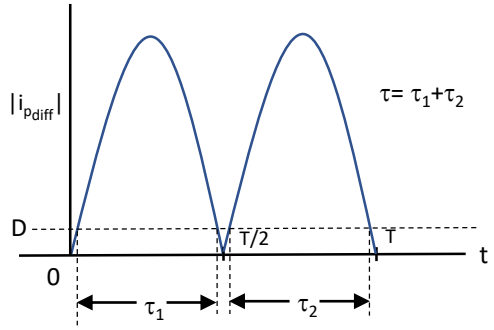

Figure 3.14: Base angle τ calculation for internal fault case

In this researchr, τ is calculated by comparing $|i_{p_{diff}}|$ with a small positive threshold D as shown in Figure 3.14. The calculation accuracy depends on the value of D. An arbitrary D value can result in small τ value during low current internal fault events and this small tb value may satisfy $\tau \leq \tau_i^m$ condition and jeopardize the performance of the proposed inrush blocking scheme. Therefore, the value of D should be chosen within the range of $0 < D < D_{max}$. D_{max} is the value that results in $\tau = \tau_i^m$ during minimum fault current condition ($I_{diff} = I_{op}^{min}$). I_{op}^{min} is the minimum differential current that trigger transformer differential element (87T).

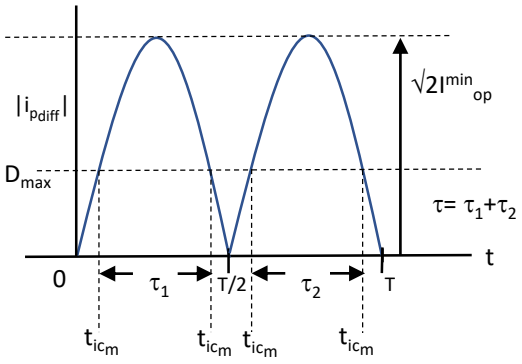

Figure 3.15: Calculation of D_{max}

Figure 3.15 illustrates the conditions which lead to derive the expression of D_{max}. $|i_{p_{diff}}|$

of internal fault current events can be expressed as Equation (3.51) where, l =[-∞, ∞].

$$|i_{p_{diff}}| = \sqrt{2} I_{min}^{op} \sin \omega t, \qquad l\pi < \omega t < (l+1)\pi \tag{3.51}$$

The conditions $\tau = \tau_1 + \tau_2 = \tau_i^m$ and $\tau_1 = \tau_2$ result the expression of t_{ic_m} as Equation (3.52). t_{ic_m} indicates the time points at when $|i_{p_{diff}}|$ curve and D_{max} line intercept each other and m= 1,2,. . . . . ,∞.

$$|t_{ic_m}| = \frac{mT \pm \tau_i^m}{4} \tag{3.52}$$

Equations (3.51) and (3.52) derive the expression of D_{max} as Equation (3.53).

$$D_{max} = \sqrt{2} I_{min}^{op} \sin \left(\omega \frac{mT \pm \tau_i^m}{4}\right) \tag{3.53}$$

Chapter 4

Bus Differential Protection Scheme

This chapter is written based on [75] and presents a novel bus differential protection scheme which provides complete immunity against the mis-operation due to CT saturation during close-in external faults and ehanced sensitivity for internal faults. The proposed scheme incorporates a fault discrimination algorithm using Partial operating current (POC) characteristic which is capable of discriminating high current internal and external faults even with CT saturation. A supervision technique based on CT saturation detection is also included in the scheme design to increase the sensitivity of the proposed relaying scheme for very high impedance internal faults. A relay model is built in Matlab platform based on the proposed scheme and the performance is validated using a transmission network simulated in Electro-Magnetic Transient Program (EMTP) for all possible fault scenarios. Documented results show the improved performance of the proposed scheme when compared to traditional bus differential scheme in terms of reliability, sensitivity, selectivity and speed. Moreover, the proposed scheme is simple and has less computational burden.

4.1 Scheme Design

The proposed scheme detects faults based on dual slope restraint characteristic and uses POC characteristics as well as the supervision of CT saturation detection algorithm to discriminate between internal and external faults. The block diagram of the proposed bus differential scheme is shown in Figure 4.1. The scheme has five functional blocks including Data Processor, Fault Detector, Fault Discriminator, CT Saturation Detector, and Trip Logic unit. Fault Detector block detects faults using current mismatch and toggles a logic bit "F". Fault Discriminator block discriminates between internal and external faults and outputs a logic bit "IEF". CT Saturation block detects any sort of CT saturation and operates a logic bit "SAT". Using logic bits "IEF", "F", and "SAT" from the previous three blocks, Trip Logic

Unit declares "TRIP". Details of each block are presented in the following sub-sections.

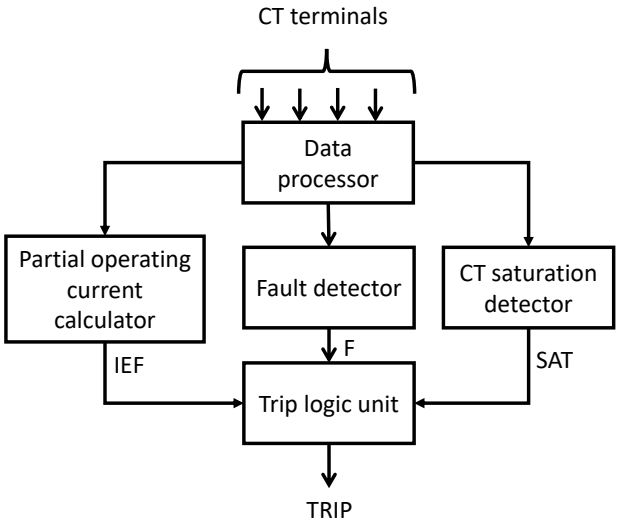

Figure 4.1: Basic block diagram of the proposed relay

4.1.1 Data Processor

The CT secondary currents are analog signals and they are sampled in a particular sampling rate to convert them into discrete signals. In this relay model, the sampling frequency is 200 samples per cycle. From these discrete signals, complex phasor values are extracted by using Discrete Fourier Transform (DFT) technique with a one cycle window as shown in Equation (4.1) [98] .

$$I(w_k) = \sum_{n=0}^{N-1} i(t_n) exp(-j w_k t_n) \tag{4.1}$$

In Equation (4.1): $i(t_n)$ is discrete current signal and I_{w_k} is the desired phasor of k^{th} harmonic component. k, n, w, t_n and N represents harmonic number, sample number, angular frequency at k^{th} harmonic, time of n^{th} sample and sampling rate respectively.

4.1.2 Fault Detector

The false operating current always exists even in normal operating conditions due to the mismatch of CT ratio and burden. This false operating current is proportional to the restraint current. To address these issues, dual-slope percentage restraint characteristic [7,84] as shown in Figure 4.2 is included in the scheme design to detect faults or abnormal conditions.

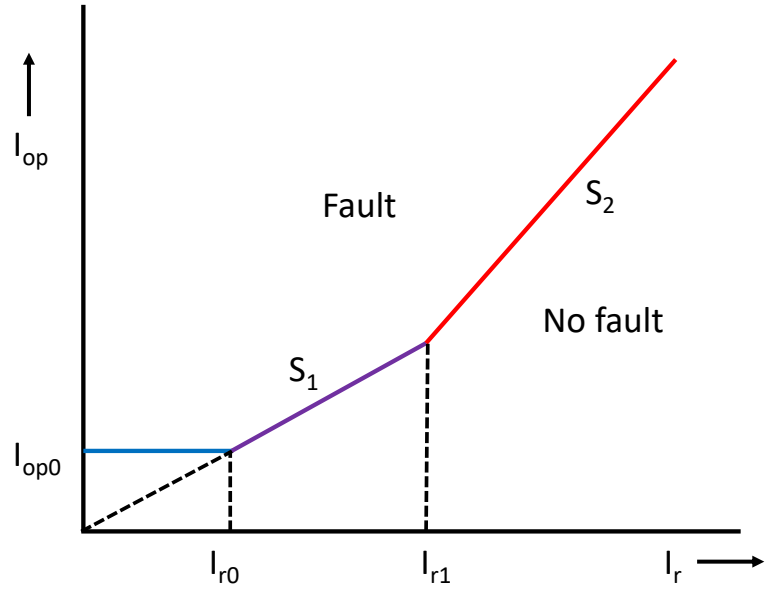

Figure 4.2: Operating characteristics of fault detector

The operating current I_{op}, and restraint current I_r are defined in Equations (4.2) and (4.3).

$$I_{op} = |I_1 + I_2 + ... + I_n| \tag{4.2}$$

$$I_r = 0.5[|I_1| + |I_2| + ... + |I_n|] \tag{4.3}$$

In Equations (4.2) and (4.3): n is the number of terminals connected to the busbar and $I_1 - I_n$ represent corresponding terminal current phasors.

Depending on the value of I_r, the characteristic of percentage restraint fault detector

shown in Figure 4.2 can be divided into three regions including $0 < I_r < I_{r0}$ (Region 1), $I_{ro} < I_r < I_{r1}$ (Region 2), and $I_r > I_{r1}$ (Region 3). The fault detection principle of each of the three regions is defined by Equations (4.4), (4.5), and (4.6), respectively.

Region 1:

$$I_{op} > I_{op0} \tag{4.4}$$

Region 2:

$$I_{op} > S_1(I_r - I_{r0}) + I_{op0} \tag{4.5}$$

Region 3:

$$I_{op} > S_2(I_r - I_{r1}) + S_1(I_{r1} - I_{r0}) + I_{op0} \tag{4.6}$$

In Equations (4.4), (4.5), and (4.6): S_1 and S_2 are the first slope and second slope of the curve shown in Figure 4.2. The value of S_1 can vary from 0.1 to 0.7 [84]. The value of S_2 must be higher than S_1 can vary from 0.2 to 0.8 [84]. I_{op0}, I_{r0} and I_{r1} represent minimum operating current pickup, first transition point and second transition point respectively.

The fault detector sets fault detection bit "F" to logic 1 only when the system operating point reaches above the curve shown in Figure 4.2.

4.1.3 Fault Discriminator

The fault discrimination algorithm included in the scheme is design based on the characteristic metrics of the POCs of a protection zone. Partial Operating Currents (POCs) are the resultants of cumulative vector addition of terminal current phasors. For an n-terminal busbar protection zone, the terminal current phasors $I_1, I_2, I_3, ..., I_n$ yield $(n-1)$ POCs as described in Equation (4.7).

$$I_{op(k)} = I_{op(k-1)} + I_{k+1} \tag{4.7}$$

In Equation (4.7): $k = 1, 2, ..., (n-1)$ with initial condition $I_{op(0)} = I_1$. $I_{op(k-1)}$ and I_{k+1} represent two *input currents* of $I_{op(k)}$.

The POC characteristic shows that each resultant partial operating currents for a protection zone is greater than the larger one of its two input currents during internal faults as described in Equation (4.8). However, for normal operation and external fault conditions irrespective of CT saturation, the statement of Equation (4.8) is violated. Equation (4.8) is a mathematical function to discriminate internal and external faults, which eliminates the computational burden of phase angle meaurement.

$$|I_{op(k)}| > max(|I_{op(k-1)}|, |I_{k+1}|) \qquad for\ k = 1, 2, ..., (n-1) \tag{4.8}$$

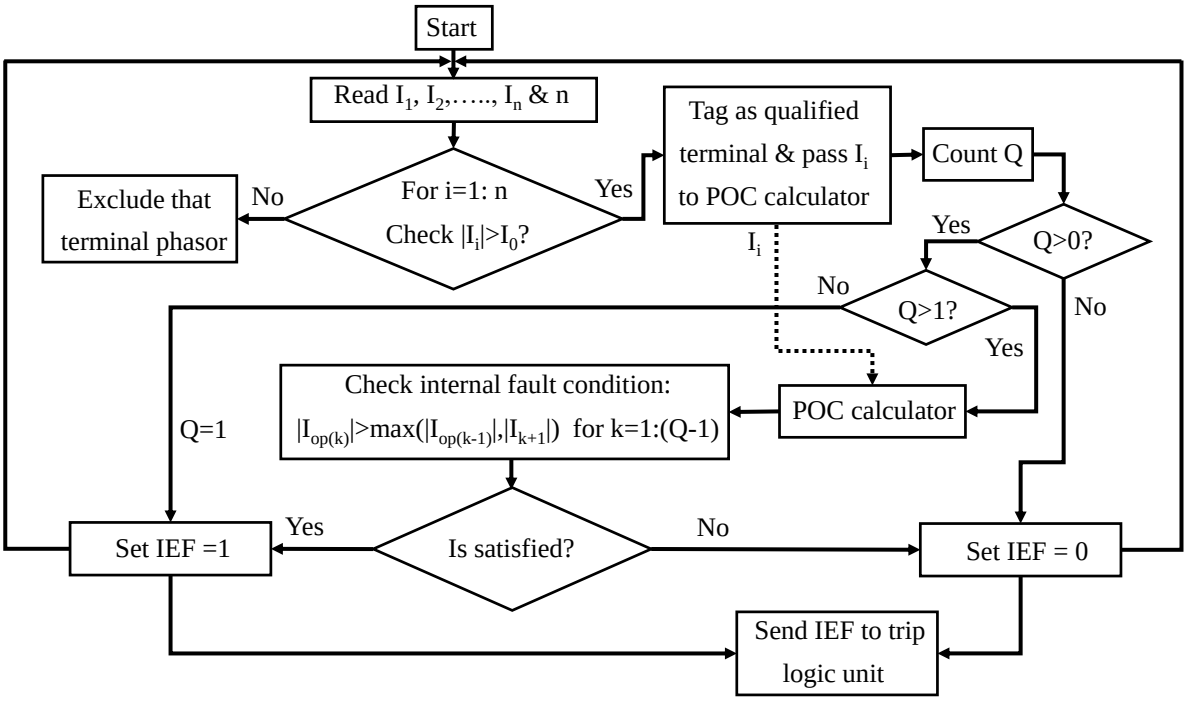

Figure 4.3: Flow chart of the POC algorithm

In practical applications, not all the elements connected to a protection zone have active sources behind them or any line can be opened from far end. Small current may continue to flow on these passive elements or on an opened line during fault. Therefore, current through the terminal less than a specific set value I_0 is considered zero current and excluded from partial operating current phasor calculation. The value of I_0 depends on the charging current

of longest line connected to the zone. A terminal of busbar is known as "qualified terminal" when current magnitude of that terminal is greater than I_0. For n-terminal busbar, if number of qualified terminals is Q then Equation (4.8) can be re-written as Equation (4.9).

$$|I_{op(k)}| > max(|I_{op(k-1)}|, |I_{k+1}|) \qquad for\ k = 1, 2, ..., (Q-1) \tag{4.9}$$

Equation (4.9) is refered as "internal fault condition" and used to design the fault discriminator. The flow chart of fault discriminator algorithm is presented in Figure 4.3 and summarized as follows:

- Read terminal number n and all terminal phasors $I_1, I_2, ..., I_n$ as input.
- Check the magnitude of each terminal phasor. If the magnitude of a terminal phasor is greater than I_0, then tag it as "qualified terminal" and pass to POC calculator; otherwise exclude it from POC calculation.
- Count the number of qualified terminal currents (Q). If $Q > 0$, go to next step; otherwise set internal fault bit "IEF" to 0 and return to first step. $Q = 0$ indicates all terminal current phasors are zero or close to zero, which means no fault at busbar.
- If $Q > 1$, go to next step; otherwise (Q=1) set internal fault bit "IEF" to 1 and return to first step. $Q = 1$ means only one terminal current phasor is high and all others are zero or close to zero, which indicates that there is a definate internal fault at busbar.
- Calculate POCs from qualified terminal current.
- Check the "internal fault condition" : $|I_{op(k)}| > max(|I_{op(k-1)}|, |I_{k+1}|)$ for $k = 1 : (Q-1)$.
- If POC characteristics satisfy "internal fault condition", set internal fault bit "IEF" to logic 1, otherwise set internal fault bit "IEF" to logic 0. Then return to first step.
- Send internal fault bit "IEF" to trip logic unit.

4.1.4 CT Saturation Detection

The proposed method to detect CT saturation during external bus faults which uses alienation coefficient of two instantaneous current signals found from the two-terminal equivalent model of the busbar. The alienation coefficient is the indicator of non-similarity between two current signals [21] and during external faults alienation coefficient becomes high only in the event of CT saturation. CT does not saturate instantaneously with inception of external faults. According to [95, 96], current waveforms remain undistorted at least for about 1/6 cycle before the first saturated waveform portion. The proposed method uses the time difference between fault inception and the starting of CT saturation. Alienation coefficient is used to determine the CT saturation starting time and fault inception time is calculated using first-derivative of the terminal currents. A generalized mathematical development for CT saturation detection is presented in Section 3.3.3. Figure 4.4 shows the proposed algorithm.

During internal bus faults, A_p becomes high instantaneously with the inception of faults [21]. However, A_p does not become high instantaneously with the inception of external faults. A_p is zero during external faults without CT saturation. Only the CT saturation event results in high value of A_p during external faults and CT saturation starts at least 1/6 cycle after the inception of faults [95, 96]. Therefore, A_p delays at least 1/6 cycle after fault inception to become high during external faults with CT saturation. The proposed CT saturation detection principle shown in Figure 5.5 considers a small processing time margin and declares CT saturation if the difference between fault inception time (T_1) and time instant (T_2) when A_p becomes high, is greater than or equal to 1/8 cycle or 2.04ms in 60Hz system. The time instant which satisfies the condition of Equation (3.45) for all terminal currents connected to the busbar, is the fault inception time (T_1). In this study, S is set to 2.0. T_2 is calculated by comparing A_p found from Equation (3.46) to a small positive set value A_x. In this study, A_x is set to 0.05 [21]. The output of the proposed CT saturation detector is denoted by SAT_p. SAT_p becomes high (logic 1) in the event of CT saturation during external faults.

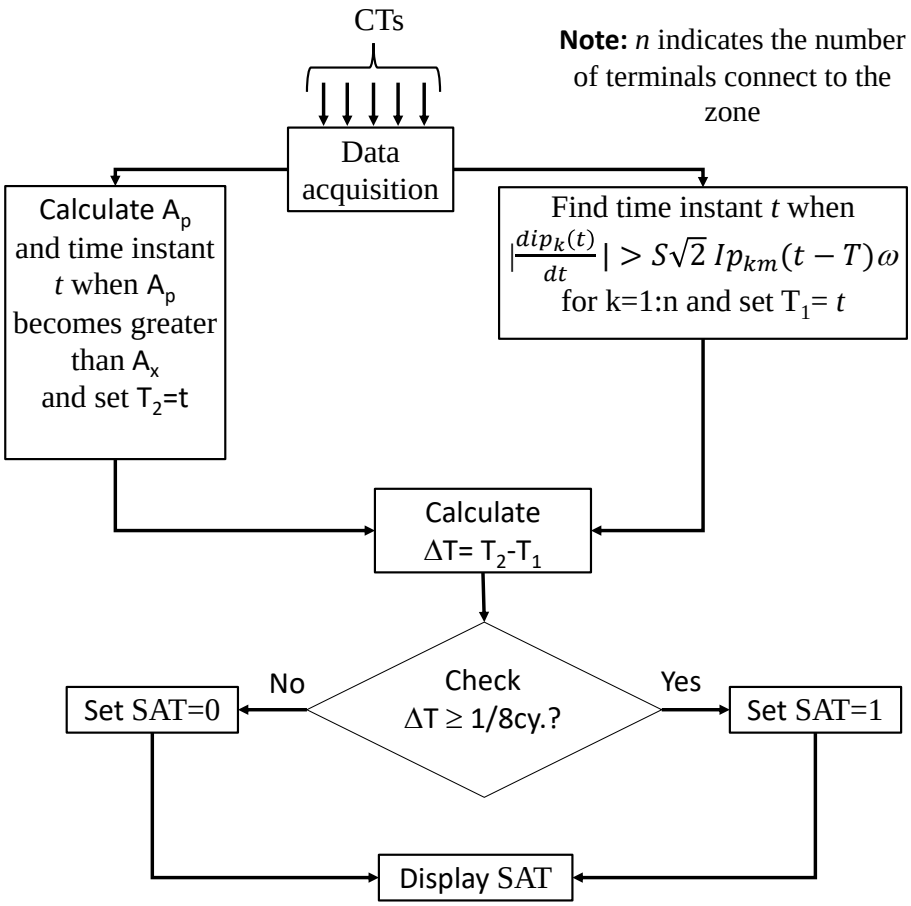

Figure 4.4: CT saturation detection algorithm

4.1.5 Trip Logic Unit

Trip logic unit is the final block of the proposed differential relaying scheme. Trip logic unit decides whether to trip or block based on the outputs of fault detector unit (F), internal-external fault discriminator unit (IEF) and CT saturation detector unit (SAT). Figure 4.5 shows the trip logic of the proposed scheme.

If both F and IEF are logic 1, the protected zone is definitely encountered by an internal fault; therefore, the proposed protection scheme issues the trip signal without any delay.

When F is logic 1 and IEF is logic 0, the zone is under either external fault with CT saturation or high impedance internal fault. To discriminate the external fault with CT saturation from high impedance internal fault, a supervision technique based on CT satu-

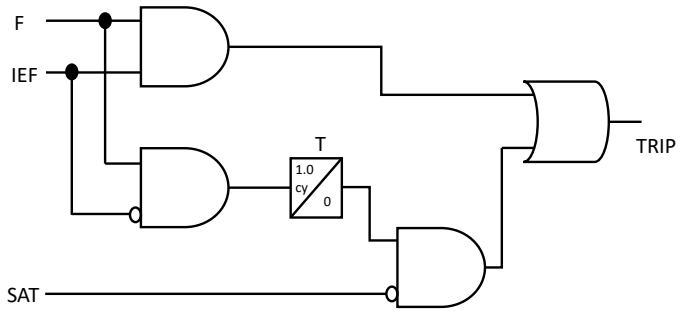

Figure 4.5: Trip logic

ration detection is used because during high impedance internal fault, fault current is low; therefore, CT remains unsaturated (SAT=0). Delayed saturation detection due to processing time of the saturation detector can cause mis-operation. Therefore, a timer T is introduced to provide 1.0 cycle time delay to ensure the correct response from saturation detector as shown in Figure 5. During high impedance internal faults, both IEF and SAT are logic 0 while F is logic 1. If these conditions persist for more than 1.0 cycle after fault detection, the proposed scheme issues trip signal for high impedance internal fault.

However, during external faults when CT saturation starts, F becomes logic 1 but IEF remains at logic 0 and within 1.0 cycle saturation detection algorithm declares CT saturation (SAT=1); therefore, the proposed differential scheme does not issue trip signal.

4.2 Testing

4.2.1 Test System and EMTP Model

A three bus 230kV system shown in Figure 4.6 is used to test the performance of the proposed bus differential protection scheme. The system has three generators, two transmission lines, and three loads at three buses. The proposed relay is applied at bus 1, where two transmission lines, one generator, and one load are connected.

The above described test system is built in EMTP. In this study, constant-parameter

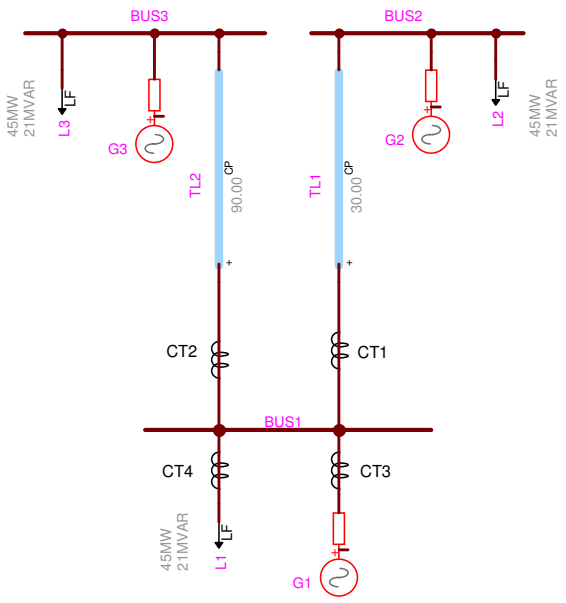

Figure 4.6: Bus Protection: Test System

distributed model is used to represent the transmission lines [99]. All generators are modeled as ideal sinusoidal voltage sources behind Thevenin impedances. The current transformers (CTs) are modeled by considering saturation impact. Figure 4.7 shows the CT model that is used in this study. This model represents an equivalent circuit built around an ideal transformer. CT parameters Rp, Lp, Ls, and inter-winding capacitance are very small which can be neglected [100]. In this study, inter-winding capacitance is neglected; however, Rp, Lp, and Ls are taken into consideration. Rs represents combined CT secondary winding resistance, lead resistance, and the CT burden.

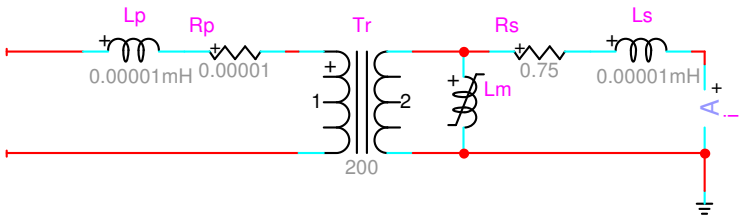

Figure 4.7: Bus Protection: Current Transformer (CT) Model

The magnetizing branch L_m is modeled as a nonlinear inductor element to include the

effect of saturation [101]. The Φ-I characteristic of the non-linear inductor is adapted from [100].

4.2.2 Relay Model and Settings

A relay is modeled in Matlab platform based on the proposed relaying scheme described in Section 4.1. The performance of the fault detector depends on four setting values including minimum pickup (I_{op0}), slope 1 (S_1), slope 2 (S_2), and second transition point (I_{r1}). Table 4.1 shows the settings that are used in this study.

Table 4.1: Bus Protection: Setting Values for Fault Detector

I_{op0} (pu)	S_1	S_2	I_{r1} (pu)
0.5	0.2	0.3	5

The calculated charging current of the longest transmission line (90km) of the test system is 0.17 pu considering 0.47A/km charging current for 230kV overhead transmission line [102]. The threshold value I_0 for fault discriminator is set to 0.4 pu (250 of 0.17 pu). All calculation presented in this paper is considering the MVA base of 100MVA.

4.2.3 Results and Discussions

As a power system element, a busbar can be affected by any type of practical faults including Phase-Ground (PG), Phase-Phase (PP), Phase-Phase-Ground (PPG), Three-Phase (PPP) and Three-Phase-Ground (PPPG). All types of practical internal faults listed in Table 4.2 are simulated using the developed EMTP model by varying the fault impedance (Z_f). Measured currents recorded by EMTP are used as input to the Matlab relay model. For each type of internal fault, eighteen (18) separate cases are studied considering both CT saturation and without CT saturation conditions, and using different fault impedance values ranging from 0.01Ω to 500Ω. Tripping Time (TT) is recorded for each case. A fault for Z_f >500Ω creates negligible operating (differential) current and therefore fault detector does not detect this fault.

Table 4.2: List of internal faults considered to test the proposed method

Fault Type	Fault Location	CT Saturation	Z_f in Ω	Total Cases	Min. TT (ms)	Max. TT (ms)
PG	Internal	Yes/No	0.01-500	18	8.8	26.67
PP	Internal	Yes/No	0.01-500	18	8.8	26.67
PPG	Internal	Yes/No	0.01-500	18	8.8	26.67
PPP	Internal	Yes/No	0.01-500	18	8.8	26.67
PPPG	Internal	Yes/No	0.01-500	18	8.8	26.67

Table 4.3: List of external faults considered to test the proposed method

Fault Type	Fault Location	CT Saturation	Z_f in Ω	Total Cases	Relay Trip
PG	External	Yes	0.01	3	No
PP	External	Yes	0.01	3	No
PPG	External	Yes	0.01	3	No
PPP	External	Yes	0.01	3	No
PPPG	External	Yes	0.01	3	No

External faults listed in Table 4.3 are studied considering only CT saturation condition as CT saturation causes unexpected differential current during external faults. For each type of external fault, three (3) cases are simulated by varying degree of CT saturation severity. The degree of CT saturation severity is changed by varying CT burden.

The relay model based on the proposed differential protection scheme is able to detect faults correctly for all of the test cases and issues trip signal only for internal faults irrespective of fault impedance and CT saturation. The results show that the value of fault impedance affects Tripping Time (TT). Selected three test cases are presented in this paper. They represent low-impedance internal fault, high-impedance internal fault, and external fault with CT saturation.

4.2.3.1 Phase-ground (PG) internal fault without CT saturation for $Z_f = 0.01\Omega$

Instantaneous currents (phase A only) for four branches during PG internal fault at bus 1 are shown in Figure 4.8. The branch currents i_1, i_2, i_3, i_4 during normal operation (0-50ms)

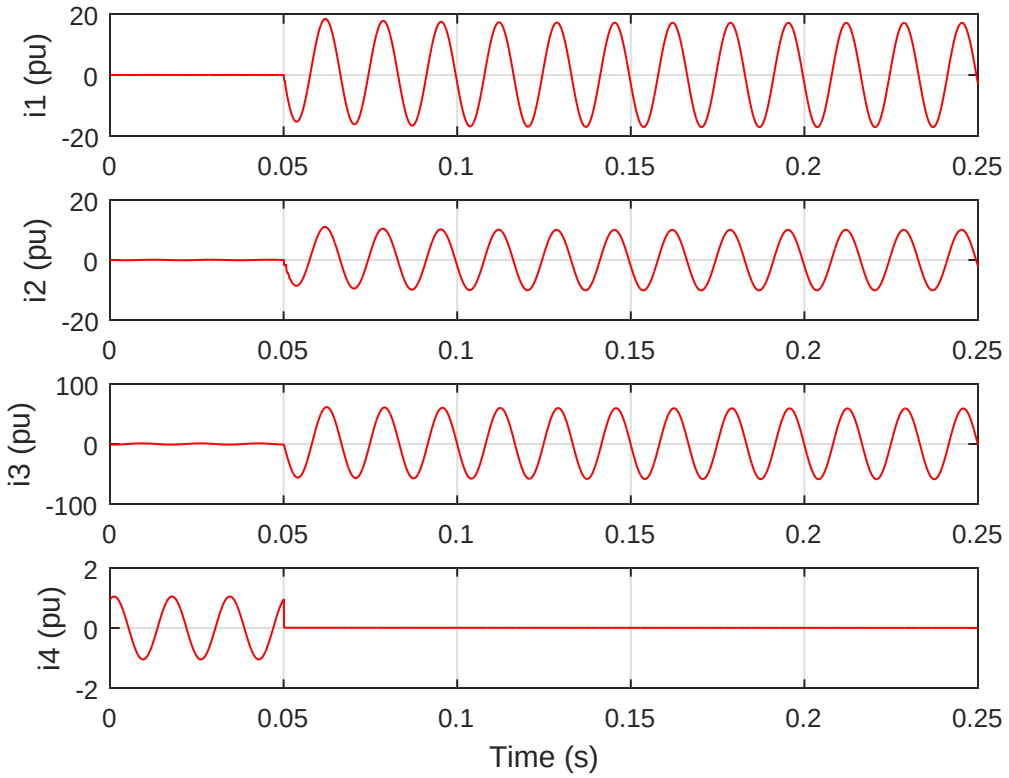

Figure 4.8: Instantaneous currents during PG internal fault with $Z_f = 0.01\Omega$

are very low in compare to faulty condition (50-250ms). The current through the load (i_4) is zero after fault inception at t=50ms as there is no active source at the other end of the load. However, currents of all other three branches are very high during fault due to the active sources behind them. The corresponding responses from the various components of the relay model for PG internal fault are shown in Figure 4.9. The output of fault detector (F) has become logic 1 (fault detected) within 1ms after fault inception. The output of fault discriminator (IEF) has become logic 1 (internal fault detected) after 8.8ms of fault inception. Consequently, the relay has issued trip command (TRIP = 1) without any delay as IEF becomes logic 1. The output of CT saturation detector (SAT) is logic 0 (no saturation) as there is no CT saturation simulated during this PG internal fault.

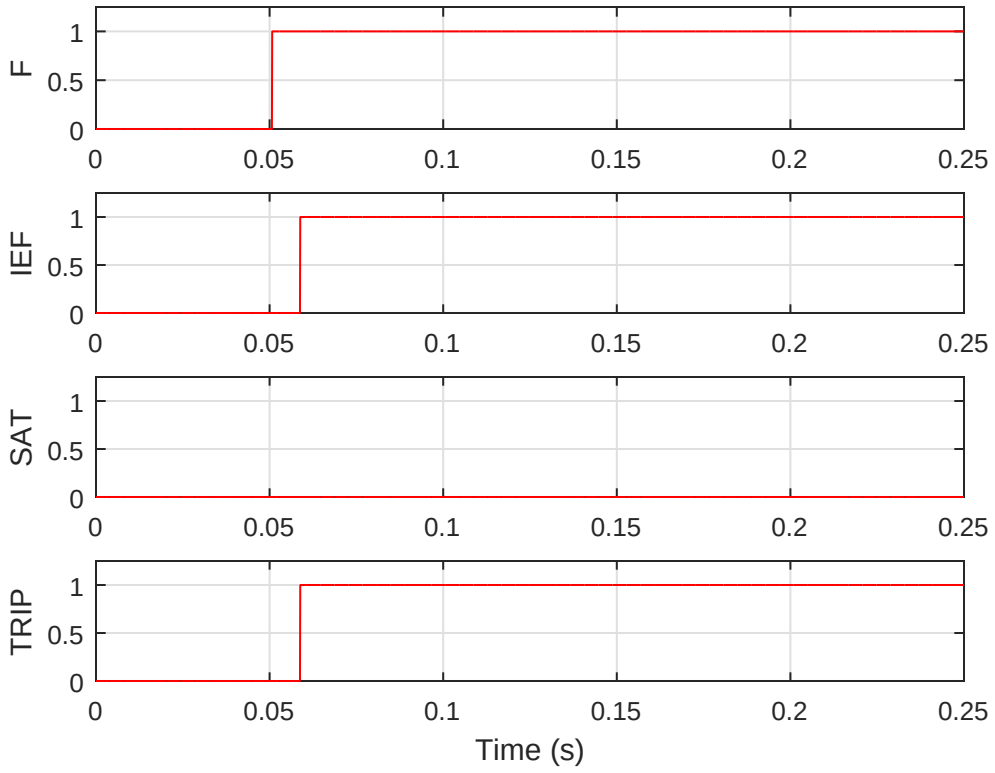

Figure 4.9: Relay responses during PG internal fault with $Z_f = 0.01\Omega$

4.2.3.2 Phase-ground (PG) internal fault with $Z_f = 500\Omega$

Instantaneous currents (phase A only) for four branches during PG high impedance ($Z_f = 500\Omega$) internal fault at bus 1 are shown in Figure 4.10. The branch currents i_1, i_2, i_3, i_4 during normal operation (0-50ms) are low in compare to faulty condition (50-250ms). After fault inception at t=50ms, the current through the load (i_4) is same as the current during normal operation because of very high fault impedance. The currents of all other three branches during fault condition are slightly higher than the currents during normal operation. The corresponding responses from the various components of the relay model for PG high impedance internal fault are shown in Figure 4.11. The output of fault detector (F) has become logical 1 (fault detected) after 10ms of fault inception. However, output of the fault discriminator (IEF) is logical 0 as the current through the load i_4 is flowing out from bus

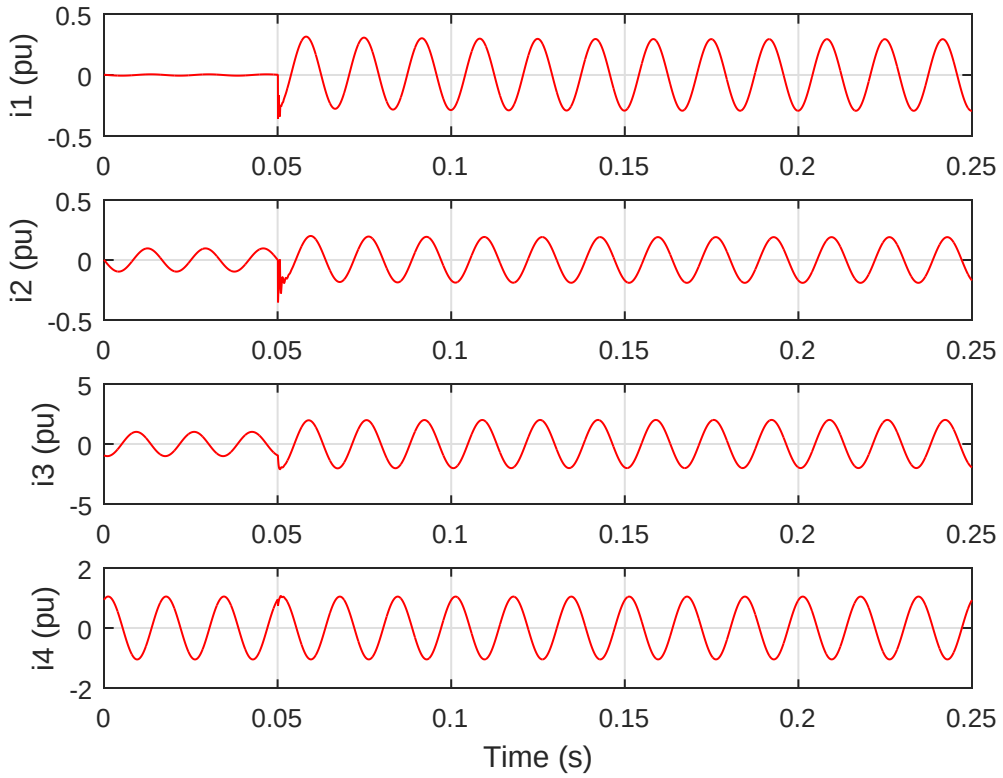

Figure 4.10: Instantaneous currents during PG internal fault with $Z_f = 500\Omega$

and its magnitude is greater than I_0. The output of CT saturation detector (SAT) is also logical 0 as there is no CT saturation during the above mentioned fault. Therefore, the relay has waited for 16.67ms (1.0 cycle) after fault detection and issued trip command (TRIP) at 26.67ms after fault inception.

4.2.3.3 Phase-phase-ground (PPG) external fault with CT saturation

Instantaneous currents (phase A only) for four branches during PPG external fault at branch 2 are shown in Figure 4.12 where i_2 is distorted due to CT saturation. The branch currents i_1, i_2, i_3, i_4 during normal operation (0-50ms) are low in compare to faulty condition (50-250ms). The load current (i_4) is zero after fault inception at t=50ms as there is no active source at the other end of the load. The currents through all other three branches are very high during fault due to the active sources behind them. The corresponding responses from

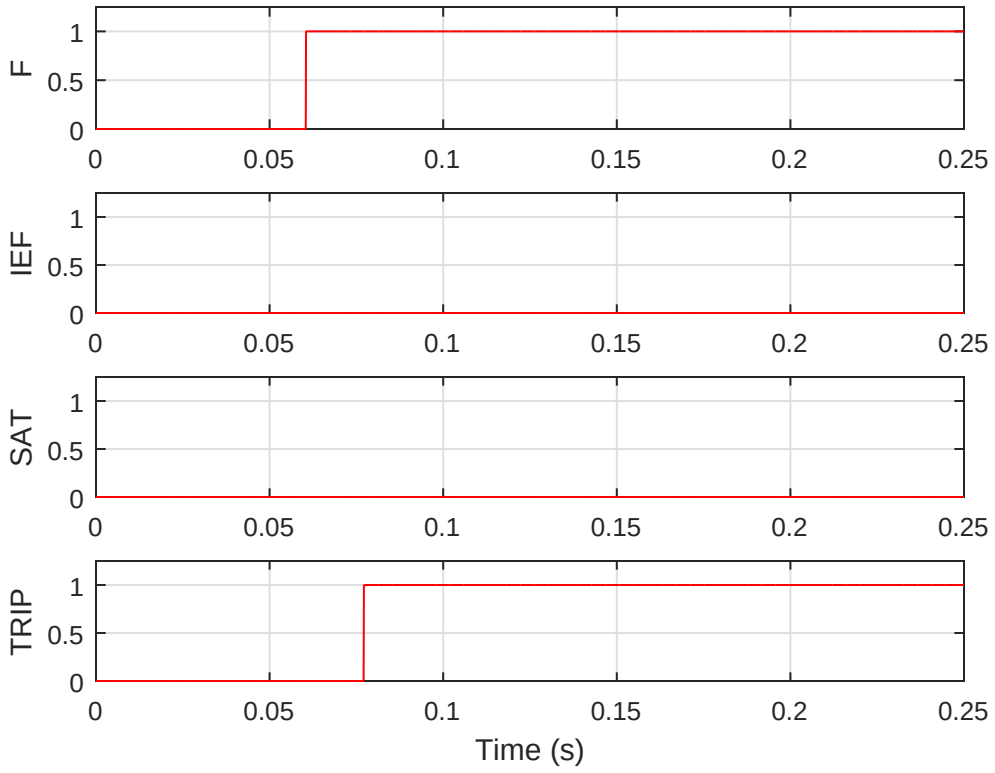

Figure 4.11: Relay responses during PG internal fault with $Z_f = 500\Omega$

the various components of the relay model for PPG external fault are shown in Figure 4.13. The output of fault detector (F) has become logical 1 (fault detected) within 2.5ms after fault inception even through the fault is incepted at out of zone (external fault). This is happened due to the resulting differential current because of CT saturation. However, output of fault discriminator (IEF) is logical 0 (external fault) as i_2 is flowing outward from the bus. The output of CT saturation detector (SAT) has become logical 1 at 2.41ms after fault detection as the CT connected to the branch 2 is saturated. Consequently, the relay has not issued trip command (TRIP) as expected.

The above simulations indicate that the proposed bus differential scheme is capable to issue trip command within sub-cycle time range after fault inception for high current internal faults (low fault impedance cases). The scheme takes longer time but less than 1.6 cycle (26.67ms) for low current internal faults (high fault impedance cases). The proposed scheme

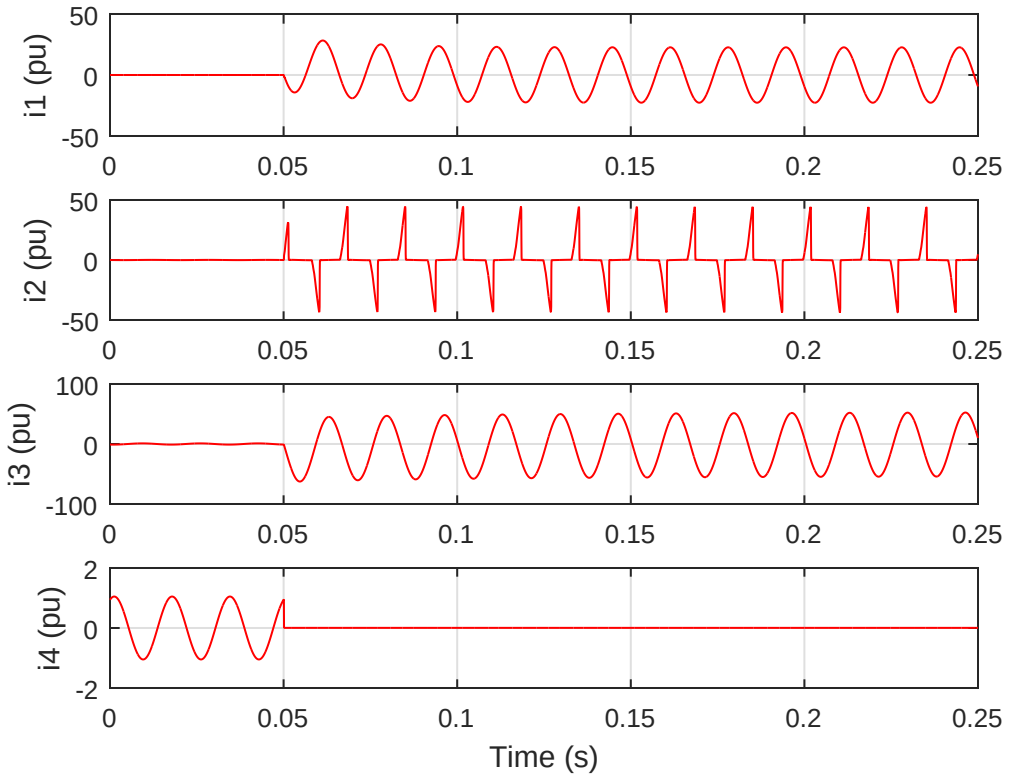

Figure 4.12: Instantaneous currents during PPG external fault with CT saturation

is reliable with 100 accuracy (92 trips out of 92 cases). The proposed scheme is also highly selective beacuse it issues trip signal only for the internal faults which create differential current greater than the set value and blocks all external faults irrespective of CT saturation (15 blocks out of 15 cases). The performance of the scheme is not affected by the degree of CT saturation severity and saturation time (fast or late saturation). The proposed scheme is also highly sensitive because it is able to detect internal faults for very high fault impedance (up to 500Ω). Moreover, the POC based fault discrimination algorithm works on simple vector addition of complex current phasors, which reduces the computational burden of the relaying system by eliminating phase estimation process.

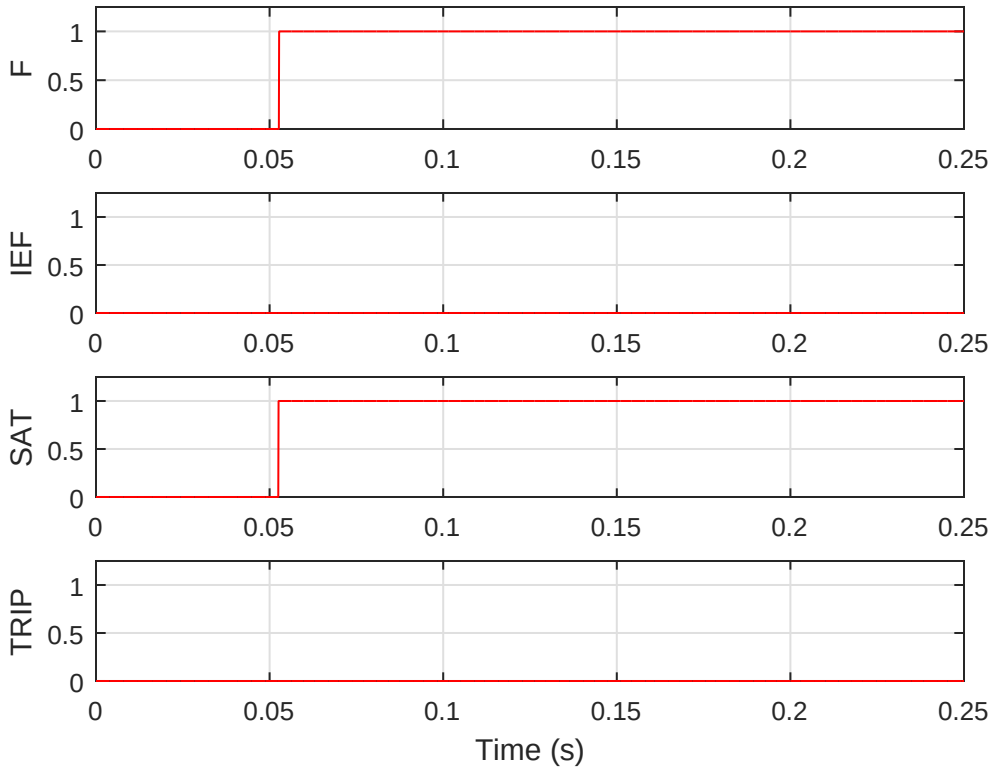

Figure 4.13: Relay responses during PPG external fault with CT saturation

4.3 Summary

This chapter presents a bus differential protection scheme to achieve complete security against CT saturation issues during close-in external faults. A new internal and external fault discrimination algorithm is included in the proposed scheme design which is working on partial operating current characteristics of a differential protection zone. To enhance the sensitivity of the proposed relaying scheme for very high impedance internal faults, a supervision technique based on newly developed CT saturation detection is incorporated. The relay model based on the proposed scheme is tested extensively using a transmission network simulated in EMTP for all possible faults under different practical scenarios such as fast CT saturation, slow CT saturation and high fault impedances. The proposed scheme is applied in a bus which is connected with active source and inactive source. The results

of the simulation study show that the proposed scheme operates correctly for all internal faults irrespective of high or low impedance and blocks the trip during external faults even for severe CT saturation conditions. Overall, the proposed relaying scheme shows enhanced performance in terms of all four functional requirements of the power system protection including reliability, selectivity, sensitivity, and speed of operation.

Chapter 5

Transformer Differential Protection Scheme

The performance of transformer differential protection is affected by Current Transformer (CT) saturation and inrush current. CT saturation during external faults and inrush current during transformer energization result in high differential (operating) current and forces a differential protection scheme to mis-trip. Existing adaptive and supervisory methods help increase the immunity against CT saturation and inrush current but degrade the sensitivity and delay the speed of relay operation during internal faults. Relay engineers need to make trade-off among security, sensitivity, and speed to set existing transformer differential protection schemes. This chapter presents a new transformer differential protection scheme based on Partial Operating Current (POC) characteristics, fast CT saturation detection, and waveform-based inrush current blocking algorithm to maximize the security against CT saturation and inrush current without sacrificing sensitivity and speed of operation during internal faults. The performance of the proposed scheme is validated by an EMTP based simulation study and results are compared with two existing transformer differential schemes. The results of the study indicate that the proposed scheme is capable of ensuring higher security, higher sensitivity, and faster relay operation.

5.1 Basics of Transformer Differential Protection

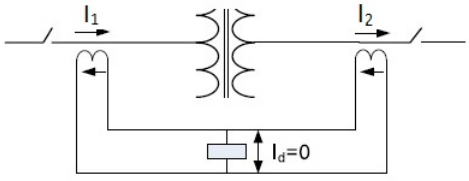

Figure 5.1: Concept of transformer protection

Figure 5.1 shows the generalized concept of transformer differential protection, where

winding or terminal currents are compared to filter out the faults. In case of transformers, incoming and outgoing terminal currents are generally not equal in magnitude as transformers are used to step up or step down the voltage. The ratio of terminal currents is inversely proportional to the voltage ratio. Moreover, the ratio of the CTs installed at different terminals can be different, which leads to magnitude mismatch of measured terminal currents. Therefore, magnitude compensation of each terminal current is necessary for transformer differential protection. Another associated challenge of transformer differential protection implementation is phase shift resulted from different winding connections. Transformer windings can be connected in Star, Delta or Zig-Zag configuration depending on the requirement of the application. Phase shift resulted from transformer configuration must be compensated before applying the differential principle. In the past, the phase shift was compensated by CT connection for old electro-mechanical relays. Modern microprocessor-based relays have internal compensation algorithms for phase shift as well as magnitude mismatch. Figure 5.2 shows the terminal current compensation block for modern microprocessor-based relays. i_{Ak}, i_{Bk} and i_{Ck} are instantaneous three phase currents of terminal k measured by CT. Magnitude compensation and phase compensation algorithms then are used to extract compensated current components (i_{AkC}, i_{BkC} and i_{CkC}). Techniques of magnitude compensation and phase compensation are described in the following subsections.

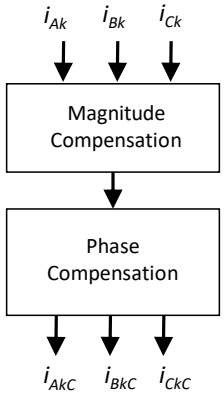

Figure 5.2: Current compensation for terminal k

5.1.1 Magnitude compensation

Magnitude compensation means scaling of terminal currents to a common base. The scaling factor is known as TAP in literature. TAP of each terminal is calculated from base MVA, rated voltage (V) in kilovolts, and the ratio of CT (CTR) installed on that terminal by Equation (5.1).

$$TAP_k = \frac{MVA * 1000}{\sqrt{3} * V_k * CTR_k} \tag{5.1}$$

In Equation (5.1), k indicates k-th terminal.

5.1.2 Phase compensation

Standard phase shift resulted from the various transformer and CT winding connections are multiple of 30 degrees. Table 5.1 shows all possible values of standard phase shift and the corresponding required phase compensation (θ) in degrees. The required phase compensation can be expressed as an index m as shown in Equation (5.2).

$$m = \frac{\theta}{30} \tag{5.2}$$

Table 5.1: Standard phase shift and compensation

Ph. shift (deg.)	0	30	60	90	120	150	180	210	240	270	300	330	360
θ (deg.)	360	330	300	270	240	210	180	150	120	90	60	30	0
m	12	11	10	9	8	7	6	5	4	3	2	1	0

Equation (5.3) represents overall winding current compensation equation for microprocessor relays. Terminal currents are scaled by TAP for magnitude compensation and $C(m)$ is the compensation matrix for the corresponding value of m to compensate phase shift.

Table 5.2: Phase compensation matrices

$$C(0) = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

$$C(1) = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}$$

$$C(2) = \frac{1}{3} \begin{bmatrix} 1 & -2 & 1 \\ 1 & 1 & -2 \\ -2 & 1 & 1 \end{bmatrix}$$

$$C(3) = \frac{1}{\sqrt{3}} \begin{bmatrix} 0 & -1 & 1 \\ 1 & 0 & -1 \\ -1 & 1 & 0 \end{bmatrix}$$

$$C(4) = \frac{1}{3} \begin{bmatrix} -1 & -1 & 2 \\ 2 & -1 & -1 \\ -1 & 2 & -1 \end{bmatrix}$$

$$C(5) = \frac{1}{\sqrt{3}} \begin{bmatrix} -1 & 0 & 1 \\ 1 & -1 & 0 \\ 0 & 1 & -1 \end{bmatrix}$$

$$C(6) = \frac{1}{3} \begin{bmatrix} -2 & 1 & 1 \\ 1 & -2 & 1 \\ 1 & 1 & -2 \end{bmatrix}$$

$$C(7) = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & -1 & 0 \\ 0 & -1 & 1 \\ 1 & 0 & -1 \end{bmatrix}$$

$$C(8) = \frac{1}{3} \begin{bmatrix} -1 & 2 & -1 \\ -1 & -1 & 2 \\ 2 & -1 & -1 \end{bmatrix}$$

$$C(9) = \frac{1}{\sqrt{3}} \begin{bmatrix} 0 & 1 & -1 \\ -1 & 0 & 1 \\ 1 & -1 & 0 \end{bmatrix}$$

$$C(10) = \frac{1}{3} \begin{bmatrix} 1 & 1 & -2 \\ -2 & 1 & 1 \\ 1 & -2 & 1 \end{bmatrix}$$

$$C(11) = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix}$$

$$C(12) = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}$$

$$\begin{bmatrix} I_{AkC} \\ I_{BkC} \\ I_{CkC} \end{bmatrix} = \frac{1}{TAP_k} C(m) \begin{bmatrix} I_{Ak} \\ I_{Bk} \\ I_{Ck} \end{bmatrix} \tag{5.3}$$

Compensation matrices for various values of m are presented in Table 5.2.

5.2 Proposed Transformer Differential Scheme

The aim of the proposed scheme is to achieve higher sensitivity and faster relay operation in case of internal faults and at the same time maintain strong security for external faults or disturbances. To achieve the targeted goal, the proposed transformer differential scheme uses the integrated logic of internal-external fault discriminator (IFT_p), phase fault detector (F_p), unbalanced fualt detector (F_{un}), CT saturation detector (SAT_p), and inrush current blocking unit (INB_p); where, p = A, B, C). The block diagram of the scheme is presented

in Figure 5.3. Each element of the scheme is described in detail in the following subsections.

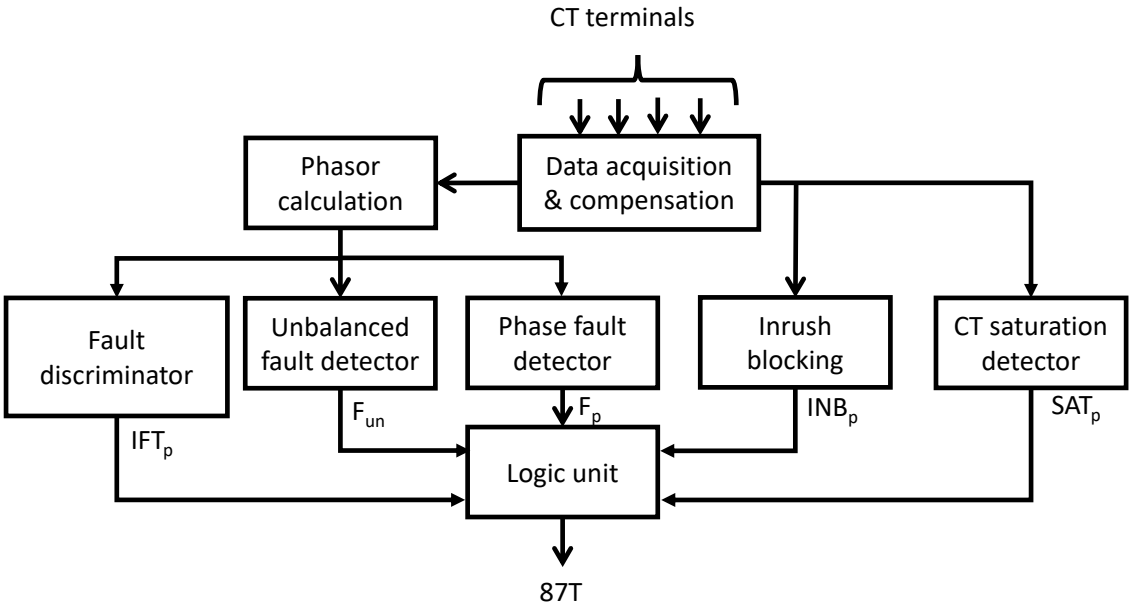

Figure 5.3: Block diagram of the proposed transformer differential protection scheme

5.2.1 Data Acquisition and Compensation

The CT secondary currents are analog signals and they are sampled in a particular sampling rate to convert them into discrete signals. In this study, the sampling frequency is considered as 200 samples per cycle. The compensation process is discussed in Section 5.1.

5.2.2 Phasor Calculation

Data acquisition and compensation unit provides compensated discrete signals. From these discrete signals, complex phasor values are extracted by using Discrete Fourier Transform (DFT) technique with a one cycle window as shown in Equation (5.1) [98].

$$I_{p_k} = \sum_{n=0}^{N-1} i_{p_k}(t_n) exp(-jwt_n) \tag{5.4}$$

In Equation (5.1): $i_{p_k}(t_n)$ is discrete current signal and I_{p_k} is the desired phasor of

fundamental component. k, n, w, t_n and N represents terminal, sample number, angular frequency, time of n^{th} sample and sampling rate respectively.

5.2.3 Phase Fault Detector

The phase fault detection is an important element of the scheme because of their sensitivity to symmetrical faults. Phase differential element is designed based on single pickup (Ip_{pk}) setting irrespective of restraint current to detect the least amount of unexpected differential current. Slope characteristic is not considered as it reduces the sensitivity [27]. Pickup (Ip_{pk}) value is set as the maximum phase current mismatch resulted in from cumulative CT errors in the nominal system operating range. The output of the phase fault detector is denoted by F_p.

5.2.4 Unbalanced Fault Detector

The proposed scheme also includes negative-sequence differential element because of its sensitivity to unbalanced faults, especially turn-to-turn faults. Negative-sequence differential element is also designed using single pickup (IQ_{pk}) value. Pickup (IQ_{pk}) value is set based on the amount of unbalance allowed by utilities. The output of unbalanced fault detector is denoted by F_{un}.

5.2.5 Fault Discriminator

The proposed internal-external fault discriminator works based on POC characteristics described in Section 3.3.2. POC algorithm calculates Partial Operating Currents (POCs) using cumulative vector addition of qualified terminal current phasors of the corresponding phase zone [74]. The qualified terminal current phasors $I_{p_1}, I_{p_2}, I_{p_3}, ..., I_{p_q}$ yield $(q-1)$ POCs as described in Equation (5.4) where, q indicates number of qualified terminals and p indicates

corresponding phase (A, B, C).

$$I_{p_{op(k)}} = I_{p_{op(k-1)}} + I_{p_{k+1}} \tag{5.5}$$

In Equation (5.4): $k = 1, 2, ..., (q-1)$ with initial condition $I_{p_{op(0)}} = I_{p_1}$. $I_{p_{op(k-1)}}$ and $I_{p_{k+1}}$ represent two *input currents* of $I_{p_{op(k)}}$.

The POC characteristic presented in [74] shows that each resultant partial operating current for a protection zone is greater than the larger one of its two input currents during internal faults as described in Equation (5.5). However, for normal operation and external fault conditions irrespective of CT saturation, the statement of Equation (5.5) is violated. Equation (5.5) is a mathematical function to discriminate internal and external faults, which eliminates the computational burden of phase angle measurement.

$$\begin{aligned} |I_{p_{op(k)}}| > max(|I_{p_{op(k-1)}}|, |I_{p_{k+1}}|) \\ for \;\; k = 1 : (q-1) \end{aligned} \tag{5.6}$$

Equation (5.5) is referred to as "internal fault condition" and used in the design of the fault discriminator. The flow chart of fault discriminator algorithm is presented in Figure 5.4 and the output is denoted by IFT_p.

5.2.6 CT Saturation Detection

The proposed method to detect CT saturation during external faults which uses alienation coefficient of two instantaneous current signals found from the two-terminal equivalent model of the differential zone. The alienation coefficient is the indicator of non-similarity between two current signals [21] and during external faults alienation coefficient becomes high only in the event of CT saturation. CT does not saturate instantaneously with inception of external faults. According to [95, 96], current waveforms remain undistorted at least for about 1/6 cycle before the first saturated waveform portion. The proposed method uses

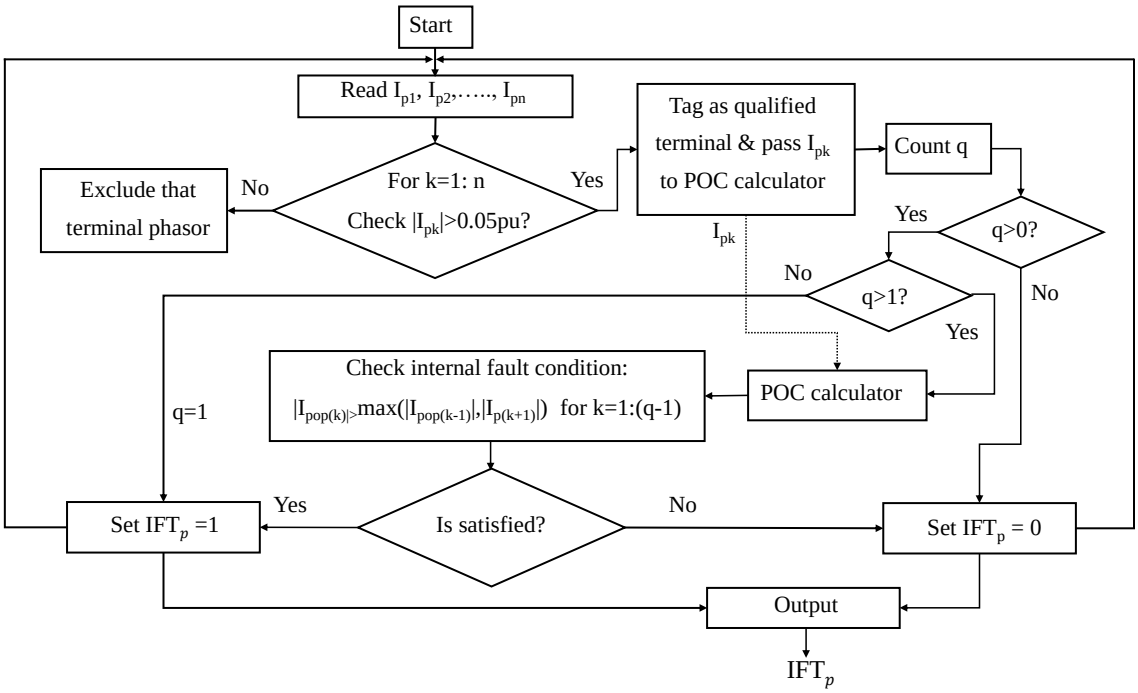

Figure 5.4: Flow chart of the POC algorithm

the time difference between fault inception and the starting of CT saturation. Alienation coefficient is used to determine the CT saturation starting time and fault inception time is calculated using first-derivative of the terminal currents. A generalized mathematical development for CT saturation detection is presented in Section 3.3.3. Figure 5.5 shows the proposed algorithm.

During internal bus faults, A_p becomes high instantaneously with the inception of faults [21]. However, A_p does not become high instantaneously with the inception of external faults. A_p is zero during external faults without CT saturation. Only the CT saturation event results in high value of A_p during external faults and CT saturation starts at least 1/6 cycle after the inception of faults [95, 96]. Therefore, A_p delays at least 1/6 cycle after fault inception to become high during external faults with CT saturation. The proposed CT saturation detection principle shown in Figure 5.5 considers a small processing time margin and declares CT saturation if the difference between fault inception time (T_1) and time instant (T_2) when A_p becomes high, is greater than or equal to 1/8 cycle or 2.04ms in 60Hz

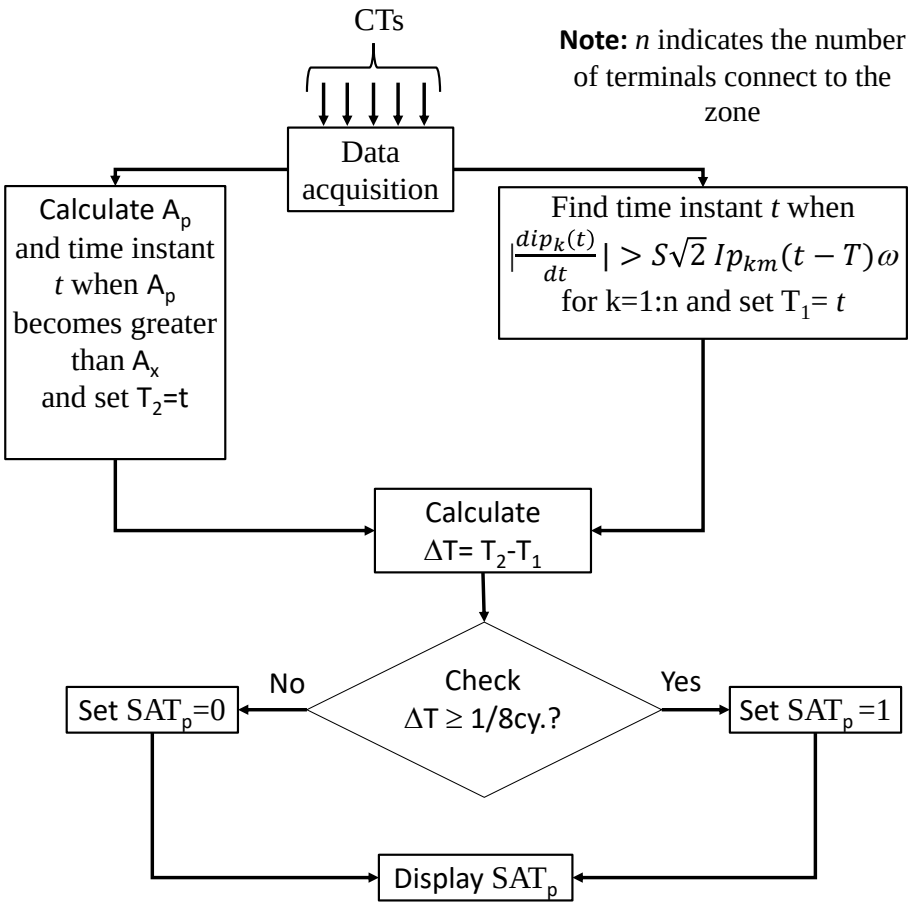

Figure 5.5: CT saturation detection algorithm

system. The time instant which satisfies the condition of Equation (3.45) for all terminal currents connected to the busbar, is the fault inception time (T_1). In this study, S is set to 2.0. T_2 is calculated by comparing A_p found from Equation (3.46) to a small positive set value A_x. In this study, A_x is set to 0.05 [21]. The output of the proposed CT saturation detector is denoted by SAT_p. SAT_p becomes high (logic 1) in the event of CT saturation during external faults.

5.2.7 Inrush Current Blocking Unit

Section 3.3.4 describes the mathematical development of the waveform-based inrush current blocking method. Based on that development, the condition for inrush current blocking is $\tau \leq \tau_i^m$, where τ and τ_i^m are the base time of the resulted $|i_{p_{diff}}|$ and maximum possible

inrush current, respectively. τ_i^m can be calculated from rated residual flux (ϕ_R) and rated saturated flux (ϕ_S) by using Equation (3.50). The proposed algorithm of the inrush current

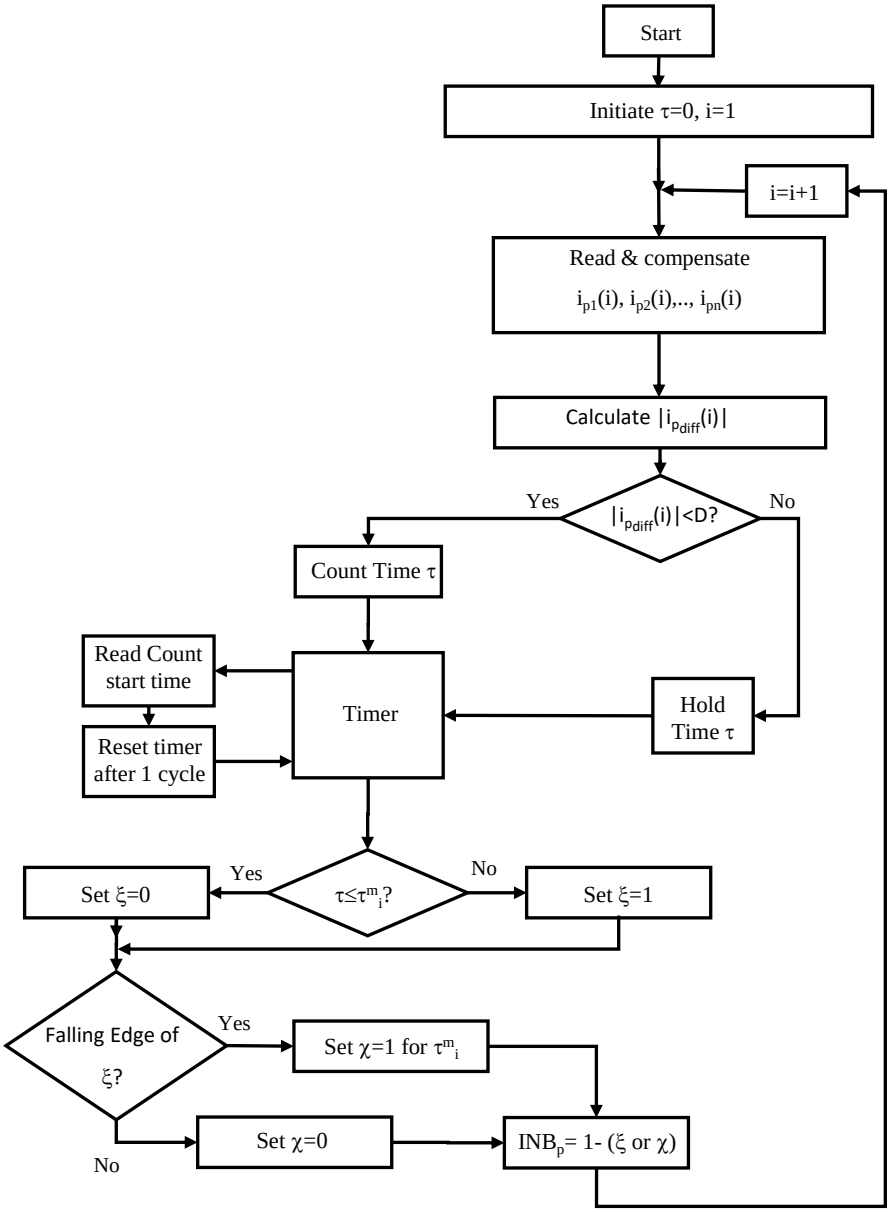

Figure 5.6: Inrush current blocking algorithm

blocking scheme is shown in Figure 5.6 which uses above-mentioned condition. The output of inrush blocking scheme is denoted by INB_p, where p represents phase. The algorithm starts by initiating a timer which is used to calculates τ. The steps of each iteration are described below:

1. Read all terminal currents for each phase differential transformer zone (n indicates number of terminals) and compensate them according to transformer ratio and configurtion.

2. Calculate absolute phase differential current, $|i_{p_{diff}}|$.

3. Timer counts time τ if $|i_{p_{diff}}| > D$; otherwise timer holds the time τ. Read time counting start time and reset timer after 1 cycle.

4. Set logic bit $\zeta = 0$ if $\tau \leq \tau_i^m$; otherwise set $\zeta = 1$.

5. Search falling edge of ζ. Set logic bit $\chi = 1$ if falling edge is found; otherwise, set $\chi = 0$.

6. Find INB_p by using equation INB_p=1-(ζ or χ).

7. Proceede to next iteration.

5.2.8 Logic Unit

The logic unit is the final block of the proposed differential relaying scheme. Figure 5.7 shows the trip logic of the proposed scheme. Trip logic unit consists of phase elements ($87T_A, 87T_B, 87T_C$) and unbalanced element ($87T_{UN}$). The phase elements work based on the outputs of fault detector (F_p) , internal-external fault discriminator (IFT_p) and CT saturation detector (SAT_p), where p = A, B, C.

If both (F_p) and (IFT_p) are logic 1, the protected zone is definitely encountered by an internal fault; therefore, the corresponding phase element becomes high without any delay.

When (F_p) is logic 1 and (IFT_p) is logic 0, the zone is under either external fault with CT saturation or high impedance internal fault. To discriminate the external fault with CT saturation from high impedance internal fault, a supervision technique based on CT saturation detection is used because during high impedance internal fault, fault current is low; therefore, CT remains unsaturated ($SAT_p = 0$). During high impedance internal faults,

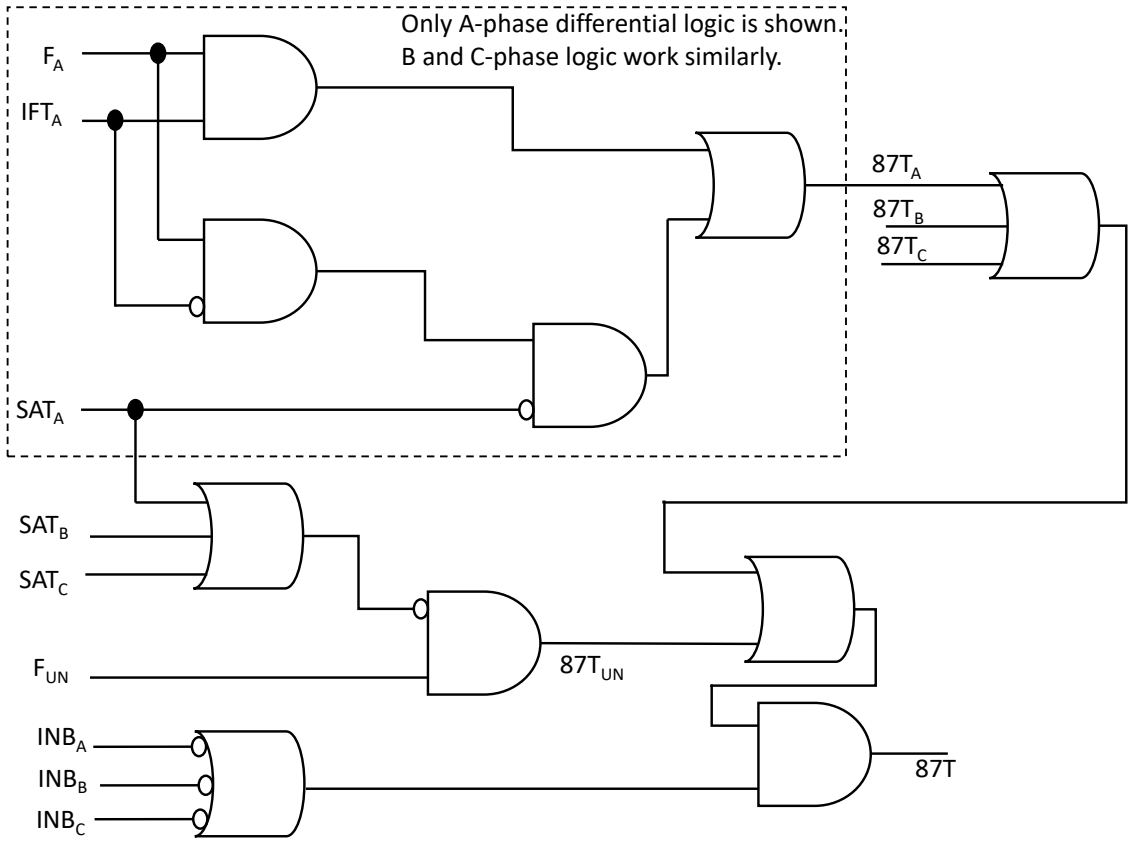

Figure 5.7: Trip logic

both (IFT_p) and (SAT_p) are logic 0 while (F_p) is logic 1 and the corresponding phase element becomes high. However, during external faults when CT saturation starts, (F_p) becomes logic 1 but (IFT_p) remains at logic 0 and the saturation detection algorithm declares CT saturation ($SAT_p = 1$); therefore, the proposed differential scheme does not issue trip signal.

The unbalanced element ($87T_{UN}$) works based on negative-sequence differential current; however, it should be blocked if there is any CT saturation.

Finally, the output of the proposed scheme ($87T$) is supervised by inrush current blocking scheme. The output of the proposed scheme becomes high, if any phase elements or unbalanced element becomes high and inrush current blocking command is not issued for any phase ($INB_p = 0$).

5.3 Testing

5.3.1 Test System and EMTP Model

The test system shown in Figure 5.8 is used to test the performance of the proposed transformer differential protection scheme. The detail of the transformer protection zone is shown in Figure 5.9. The test system parameters are presented in Appendix.

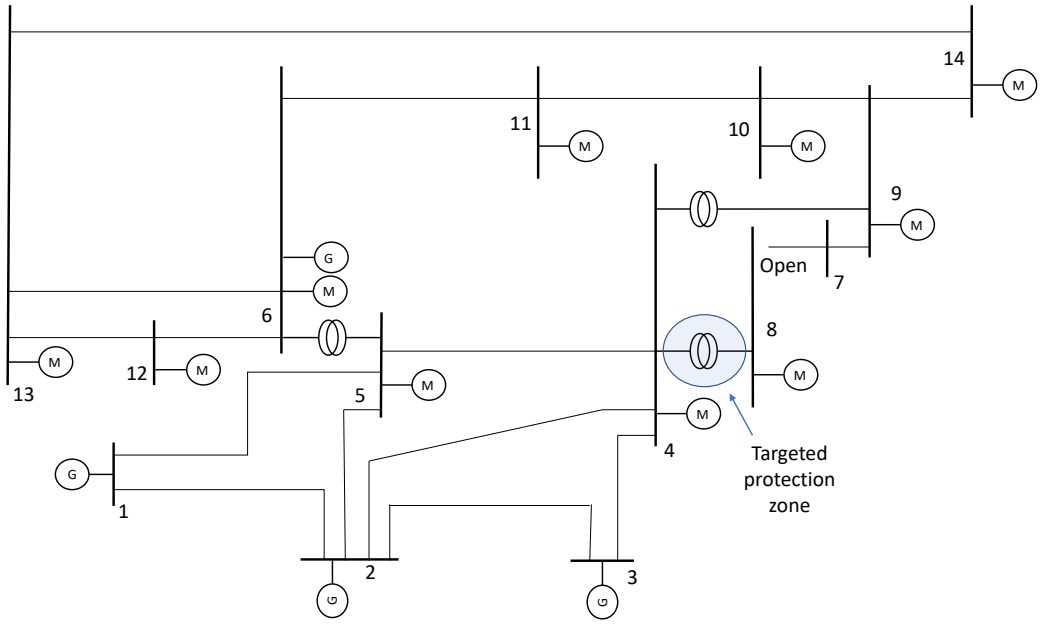

Figure 5.8: Modified IEEE 14 Bus Test System for Transformer Protection

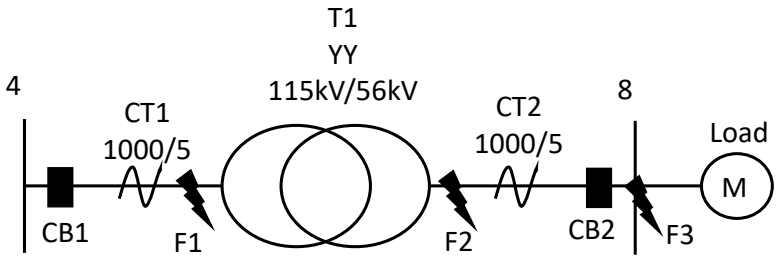

Figure 5.9: Targeted Transformer Protection Zone

The above described test system is built in EMTP.the generator is modeled as ideal sinusoidal voltage sources behind Thevenin impedances. The current transformers (CTs)

are modeled by considering saturation impact. Figure 5.10 shows the CT model that is used in this study. This model represents an equivalent circuit built around an ideal transformer. CT parameters Rp, Lp, Ls, and inter-winding capacitance are very small which can be neglected [100]. In this study, inter-winding capacitance is neglected; however, Rp, Lp, and Ls are taken into consideration. Rs represents combined CT secondary winding resistance, lead resistance, and the CT burden.

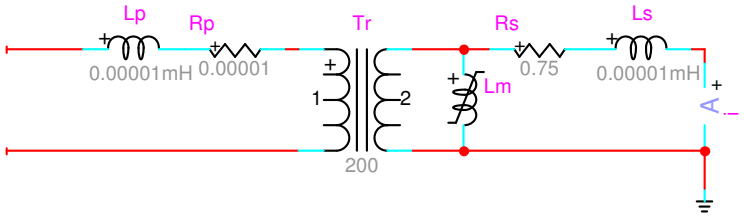

Figure 5.10: Transformer Protection: Current Transformer (CT) Model

The magnetizing branch L_m is modeled as a nonlinear inductor element to include the effect of saturation [101]. The Φ-I characteristic of the non-linear inductor is adapted from [100].

5.3.2 Relay Model and Settings

A relay is modeled in Matlab platform based on the proposed relaying scheme described in Section 5.2. The performance of the fault detector depends on four setting values including phase pickup (Ip_{pk}), unbalanced element pickup (IQ_{pk}), current base angle (β_i), and load change tolerance (S). Table 5.3 shows the settings that are used in this study.

Table 5.3: Setting Values for the Proposed Transformer Protection Scheme

Ip_{pk} (pu)	IQ_{pk} (pu)	β_i (degree)	S
0.07	0.07	240	1.2

5.3.3 Results and Discussion

To evaluate the performance of the proposed scheme, various tests were performed by applying faults in the EMTP model of the system shown in Figure 5.9 at different locations (F_1, F_2 and F_3). The performed tests comprise various internal faults including phase-ground (PG), phase-phase (PP), phase-phase-ground (PPG) and three-phase (PPP, PPPG) were simulated by varying fault resistance (R_f) to verify the sensitivity. Turn-turn (TT) faults and internal faults in presence of inrush current were also simulated. All types of external faults were simulated in various CT saturation conditions by varying CT burden. Both Ip_{pk} and IQ_{pk} were set at 0.1pu. The results of all test cases are documented in Table 5.4 and compared with two existing schemes. The two existing schemes are: ES1) Dual-slope percentage restraint characteristic with two break-points (I_{min}=0.1pu, $Break-point1$=1pu, $Break-point2$=2pu, S1=0.4 and S2=0.6) [28, 103] and ES2) Dual-slope percentage restraint characteristic supervised by phase angle comparison algorithm (I_{min}=0.1pu, S1=0.4 and S2=0.6) [10, 30].

The results of the proposed scheme for three test cases which include PG internal fault during inrush condition, PG internal fault for $R_f = 200$, and PP external fault are described below in detail.

5.3.3.1 Phase-Ground Internal Fault During Inrush Condition

The waveforms shown in Figure 5.11 indicate a phase-ground (PG) internal fault which is applied to phase-B at high-voltage (LV) side (at $F2$) of the transformer. The fault is applied at t=0.05s after transformer energization where $R_f = 200\Omega$. Figure 5.11 shows inrush current in Phase B and C for time duration t=0-0.05s at high side. The current of phase-B at high-voltage (HV) side increases instantaneously with the inception of fault, where other two phases (A and C) are not affected by fault. Transformer LV side was opened during energization; therefore, the currents are zero at LV side. F_C & F_{UN} elements are asserted at t=0.009s and F_B is asserted at t=0.012s due to inrush current (Figure 5.12). However,

Table 5.4: Transformer Protection: Comparative analysis results

Fault	Location	Expected Result	R_f (Ω)	Burden (Ω)		Operating Time (ms)		
				CT1	CT2	ES1	ES2	PS
AG	F1	T	0.1	0.75	0.75	10.1	11.4	12.3
BC	F1	T	0.1	0.75	0.75	9.39	10.72	11.8
BCG	F1	T	0.1	0.75	0.75	9.38	10.72	11.8
ABC	F1	T	0.1	0.75	0.75	9.21	10.72	11.8
ABCG	F1	T	0.1	0.75	0.75	9.21	10.72	11.8
AG	F2	T	10	0.75	0.75	10.35	NT	13.1
AG	F2	T	20	0.75	0.75	10.92	NT	13.7
AG	F2	T	50	0.75	0.75	13.1	NT	14.6
AG	F2	T	100	0.75	0.75	15.8	NT	15.34
AG	F2	T	200	0.75	0.75	16.67	NT	16.6
AG	F3	NT	0.01	0.75	10	NT	NT	NT
AG	F3	NT	0.01	0.75	25	NT	NT	NT
AG	F3	NT	0.01	0.75	50	11.42	NT	NT
AG	F3	NT	0.01	0.75	100	10.50	NT	NT
AB	F3	NT	0.01	0.75	10	NT	NT	NT
AB	F3	NT	0.01	0.75	25	NT	NT	NT
AB	F3	NT	0.01	0.75	50	11.73	NT	NT
AB	F3	NT	0.01	0.75	100	10.46	NT	NT
BCG	F3	NT	0.01	0.75	10	NT	NT	NT
BCG	F3	NT	0.01	0.75	25	NT	NT	NT
BCG	F3	NT	0.01	0.75	50	11.75	NT	NT
BCG	F3	NT	0.01	0.75	100	10.41	NT	NT
ABC	F3	NT	0.01	0.75	10	NT	NT	NT
ABC	F3	NT	0.01	0.75	25	13.50	NT	NT
ABC	F3	NT	0.01	0.75	50	12.86	NT	NT
ABC	F3	NT	0.01	0.75	100	10.67	NT	NT
ABCG	F3	NT	0.01	0.75	10	NT	NT	NT
ABCG	F3	NT	0.01	0.75	25	13.42	NT	NT
ABCG	F3	NT	0.01	0.75	50	12.85	NT	NT
ABCG	F3	NT	0.01	0.75	100	10.67	NT	NT
Inrush	-	NT	-	0.75	0.75	NT	NT	NT
Inrush-AB	F1	T	0.01	0.75	0.75	48.21	48.21	11.8
Inrush-AG	F2	T	0.01	0.75	0.75	64.13	64.13	12.3
Inrush-AG	F2	T	200	0.75	0.75	64.13	64.13	16.6
A (HV)	TT(10%)	T	-	0.75	0.75	16.66	NT	16.6
A (LV)	TT(10%)	T	-	0.75	0.75	16.67	NT	16.6

Note:- T := Trip and NT:= No Trip

all inrush blocking elements are high until t=0.0666s, therefore, no trip command is issued during this time duration. At t=0.0666s, INB_B becomes low and the trip command ($87T$) is issued (Figure 5.13).

5.3.3.2 Phase-Ground Internal Fault for $R_f = 200\Omega$

The waveforms shown in Figure 5.14 indicate a phase-ground (PG) internal fault which is applied to phase-A at low-voltage (LV) side (at $F2$) of the transformer. The fault is applied at t=0.05s where R_f is 200Ω. The current of phase-A at high-voltage (HV) side increases

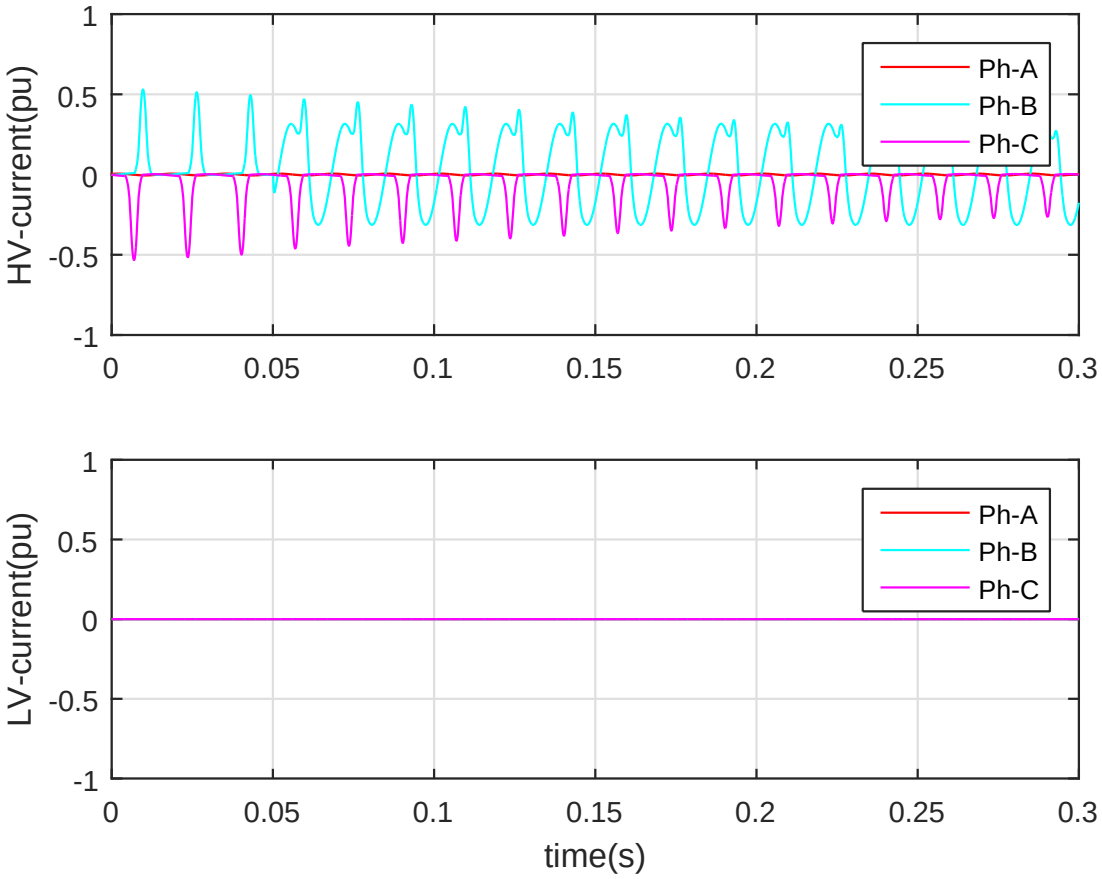

Figure 5.11: Fault currents waveforms for BG internal fault during inrush current condition

instantaneously with the inception of fault, where other two phases (B and C) are not affected. Due to high fault resistance, the current in phase-A becomes remains almost same at LV side. Only F_A & F_{UN} elements are asserted at t=0.063s because of high differential current and phase unbalance as shown in Figure 5.15. All fault discrimination and saturation elements are zero even after fault inception. Both $87T_A$ & $87T_{UN}$ elements are asserted at t=0.063 because of high differential current and phase unbalance as shown in Figure 5.16. Only one inrush detection elements (INB_A becomes low at t=0.0666s. Subsequently, $87T$ element becomes high at t=0.0666s.

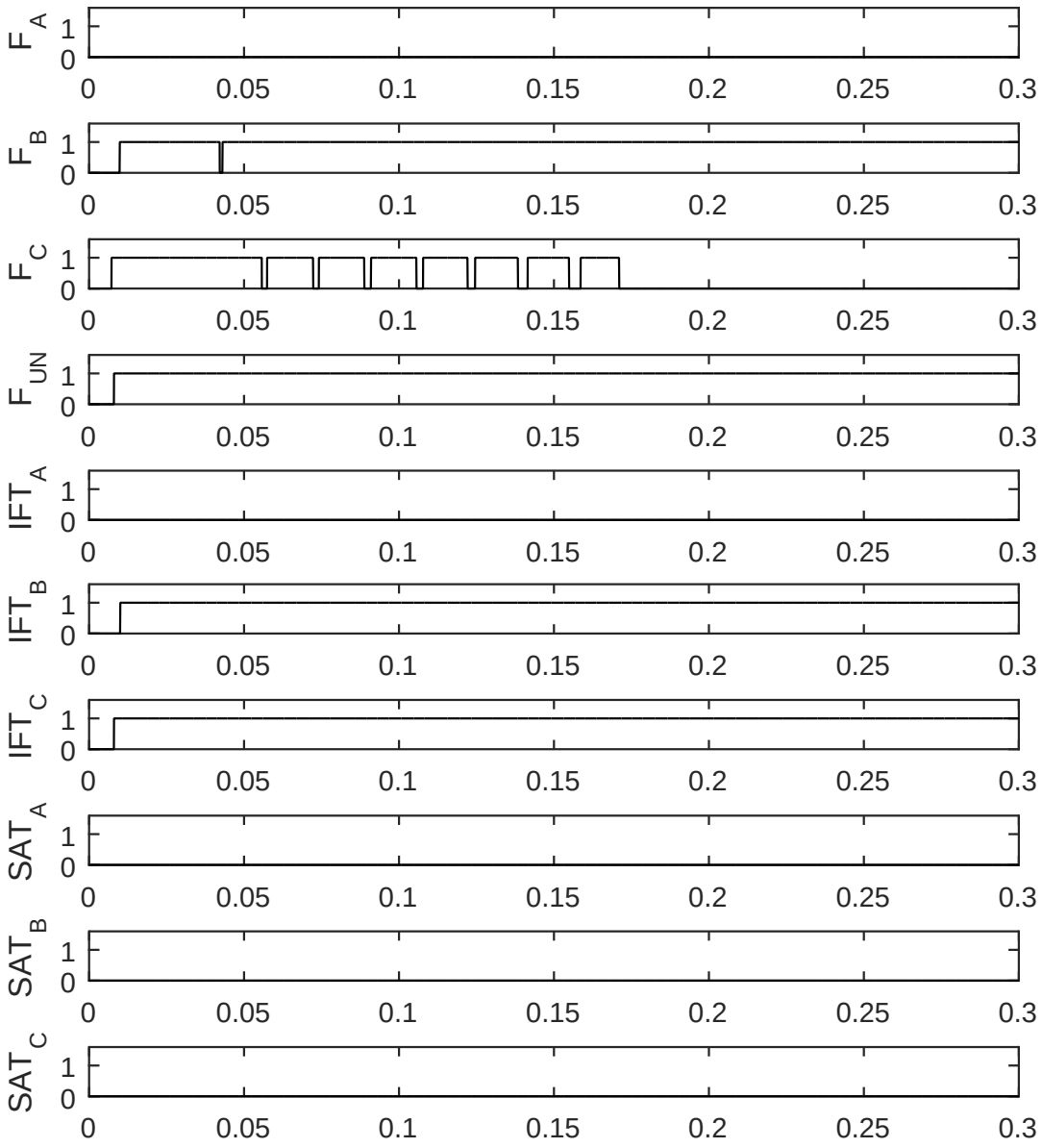

Figure 5.12: Response of proposed scheme for BG internal fault during inrush current condition part-(a)

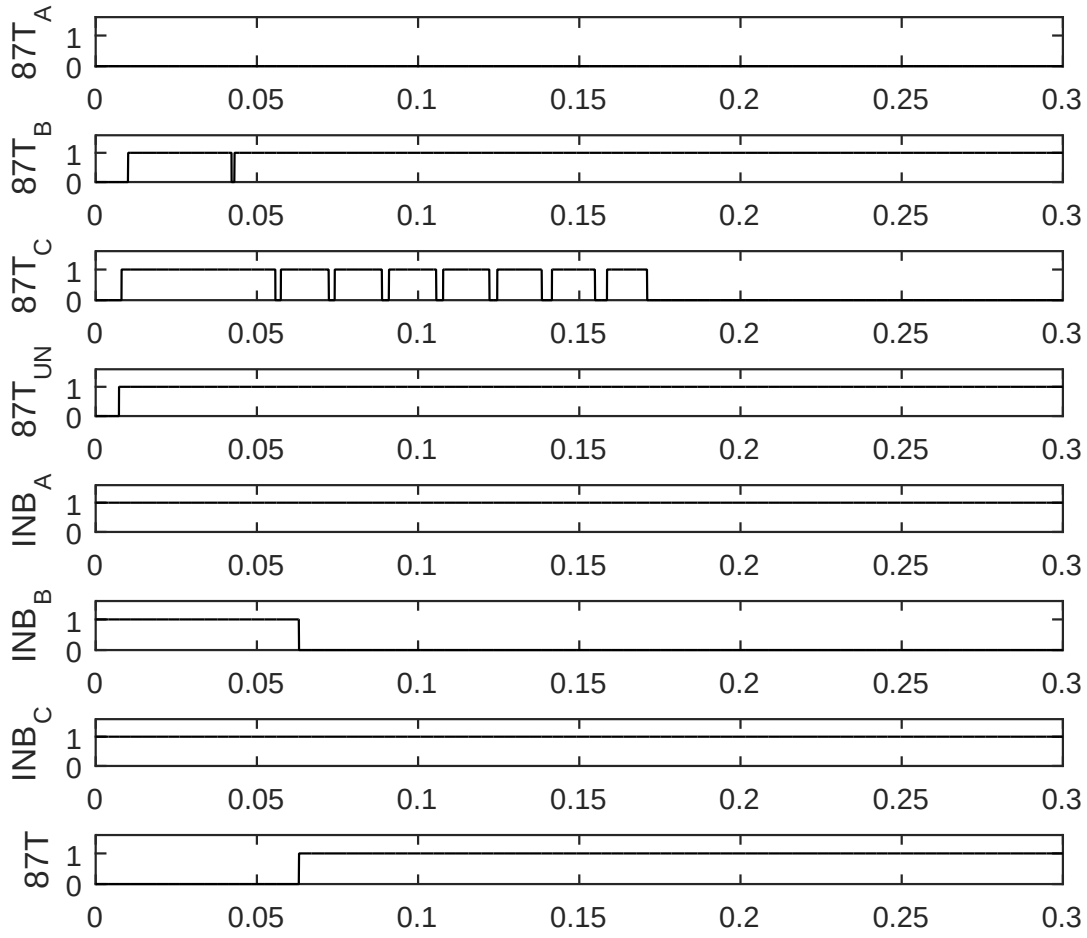

Figure 5.13: Response of proposed scheme for BG internal fault during inrush current condition part-(b)

5.3.3.3 Phase-Phase external Fault

The waveforms shown in Figure 5.17 indicate a phase-phase (PP) external fault which is applied to phase A and B at low-voltage (LV) side (at $F3$) of the transformer. The fault is applied at t=0.05s. The current of phase A and B at high-voltage (HV) and Low-side (LV) side increase instantaneously with the inception of fault, where other phase (C) is not affected. Due to high fault currents. the CTs of phase-A and B at LV side become saturated. F_A, F_B & F_{UN} elements are asserted because of high differential current and

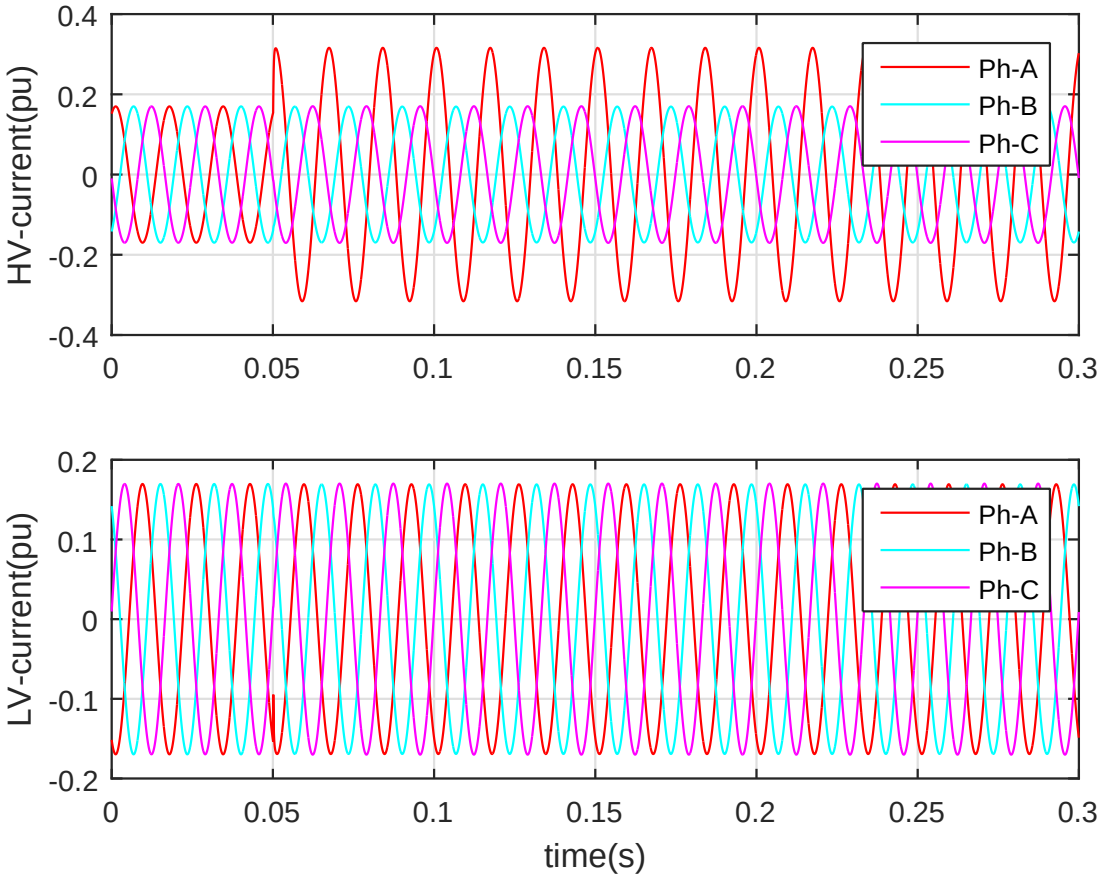

Figure 5.14: Fault currents waveforms during AG internal fault for $R_f = 200\Omega$

phase unbalance as shown in Figure 5.18. All fault discrimination are zero even after fault inception. All saturation and inrush current elements except phase-C become high as soon as the CTs start saturation (at t=0.0528s). Therefore, all differential elements are zero even as expected as illustrated in Figure 5.19.

5.3.3.4 Result Comparison

Table 5.4 shows the comparative performance of the proposed scheme (PS) with two existing schemes including: ES1) Dual-slope percentage restraint characteristic with two break-points and ES2) Dual-slope percentage restraint characteristic supervised by phase angle comparison algorithm. The performance of ES1 is affected by CT saturation and it fails to block

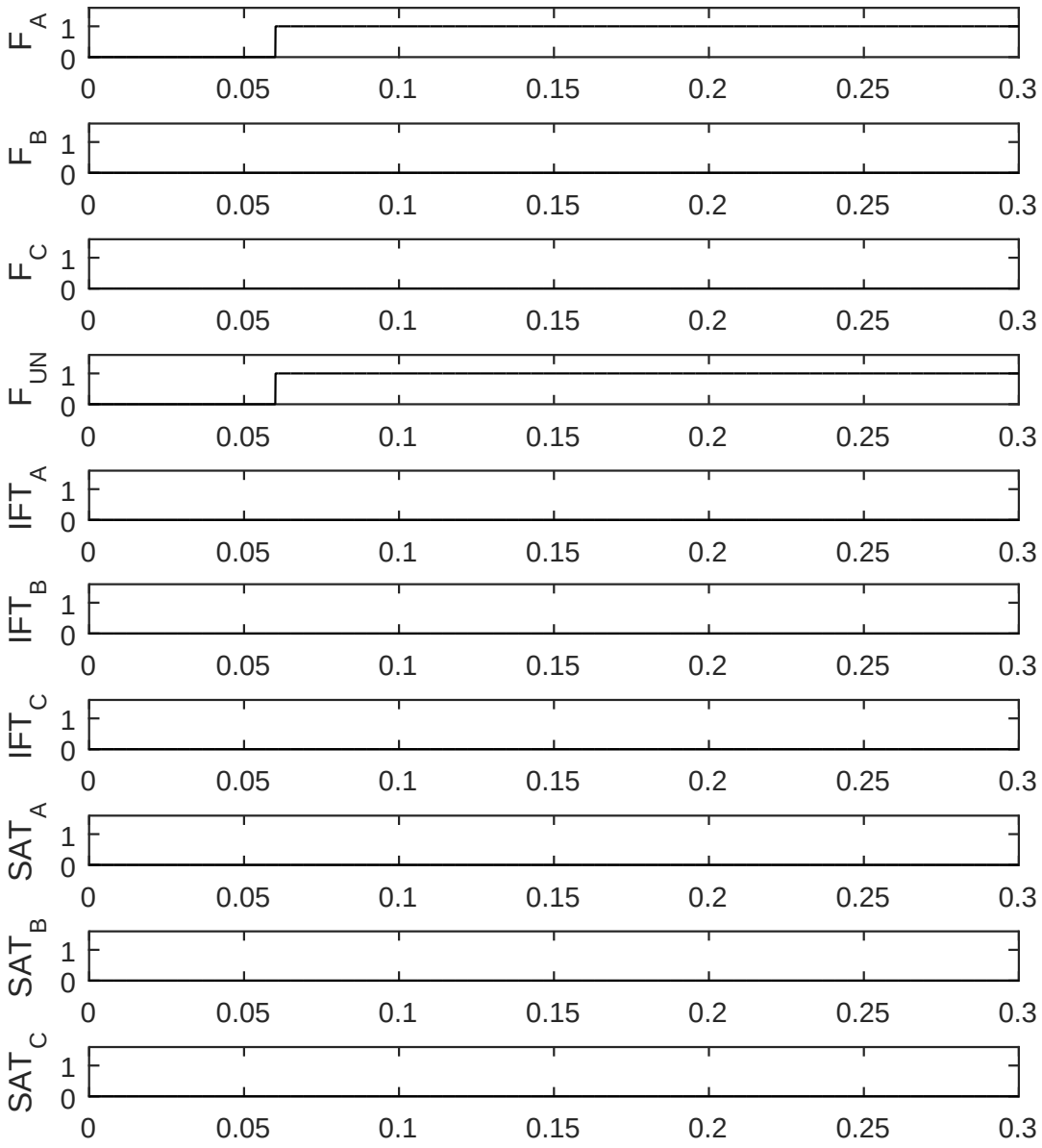

Figure 5.15: Response of proposed scheme for AG internal fault for $R_f = 200\Omega$ part-(a)

external faults for higher degrees of CT saturation as shown in Table 5.4. ES2 is unable to detect internal faults when fault resistance is high. ES2 also fails to respond correctly during turn-turn (TT) faults as indicated by last two test cases. Turn-turn faults were simulated

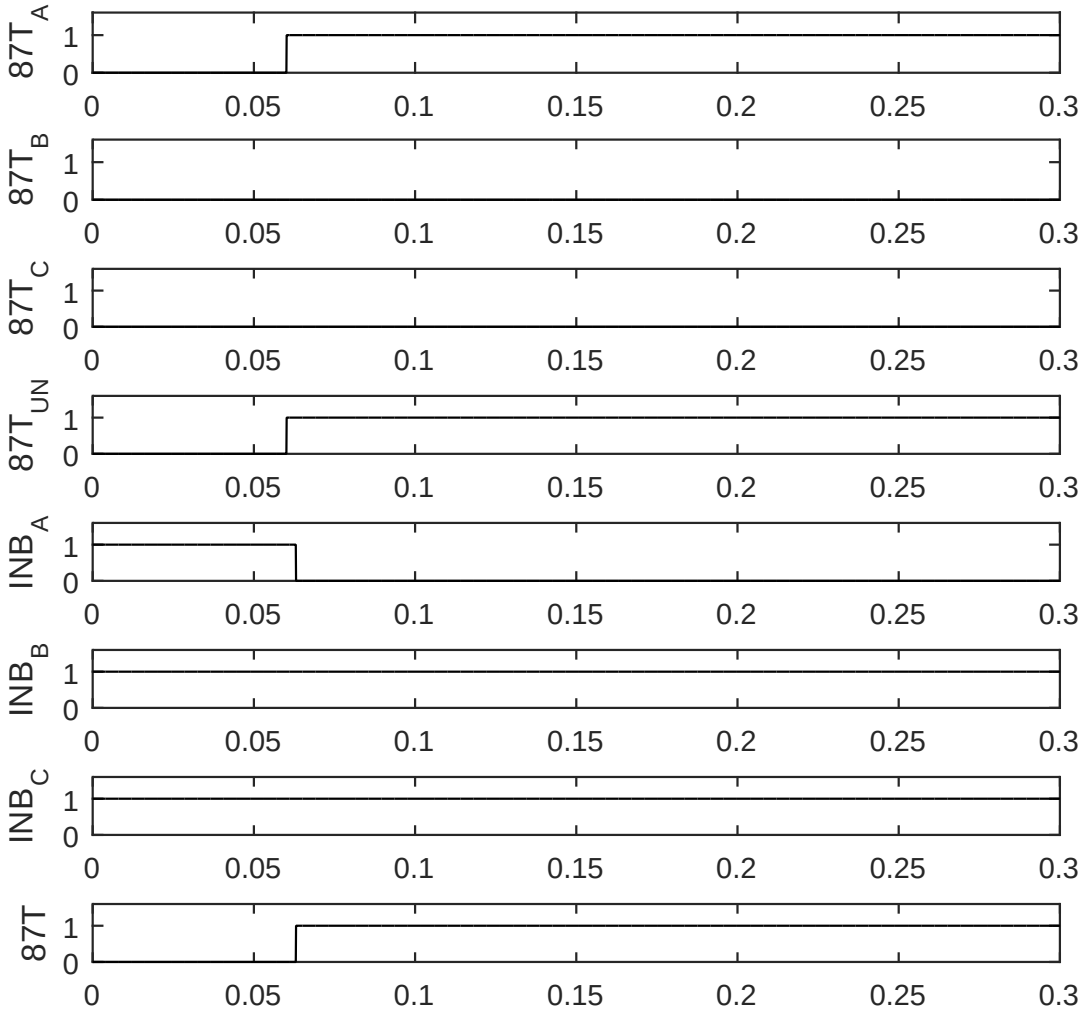

Figure 5.16: Response of proposed scheme for AG internal fault for $R_f = 200\Omega$ part-(b)

on both sides (HV & LV) by shorting 10% of phase-A winding. However, the proposed scheme (PS) performs as expected for all simulated faults irrespective of fault resistance and CT saturation conditions. The operating speed of proposed scheme (PS) is quite similar to ES1 and ES2 for low impedance internal faults. However, the proposed scheme dramtically reduces the operating time for internal faults during transformer energization.

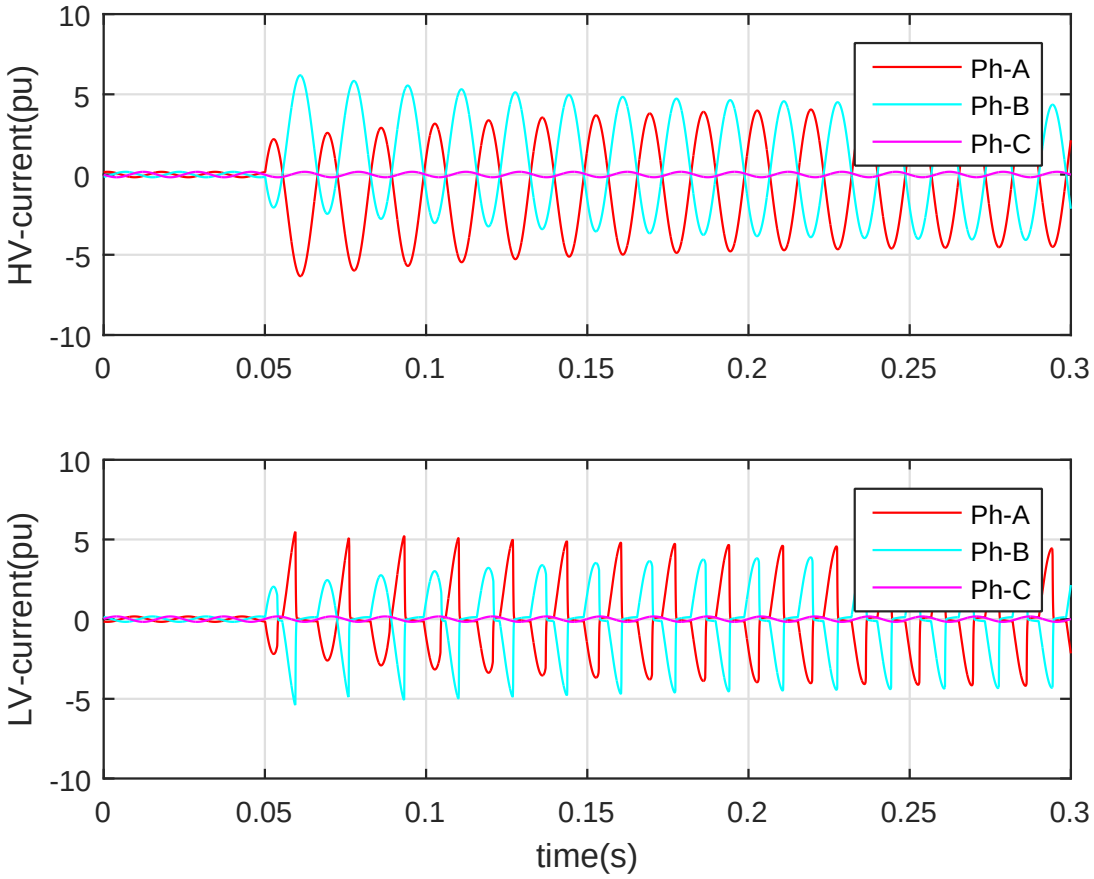

Figure 5.17: Fault currents waveforms during AB external fault with CT saturation

5.4 Summary

This chapter presents a new transformer differential protection scheme based on Partial Operating Current (POC) characteristics, fast CT saturation detection, and waveform-based inrush current blocking algorithm to maximize the security against CT saturation and inrush current without sacrificing sensitivity and speed of operation during internal faults. The scheme uses differential elements working on a single setting value instead of percentage restraint characteristics to increase overall sensitivity. Negative sequence differential element is included to detect turn-to-turn faults. The proposed scheme provides better performance in terms of security, dependibility and speed of operation.

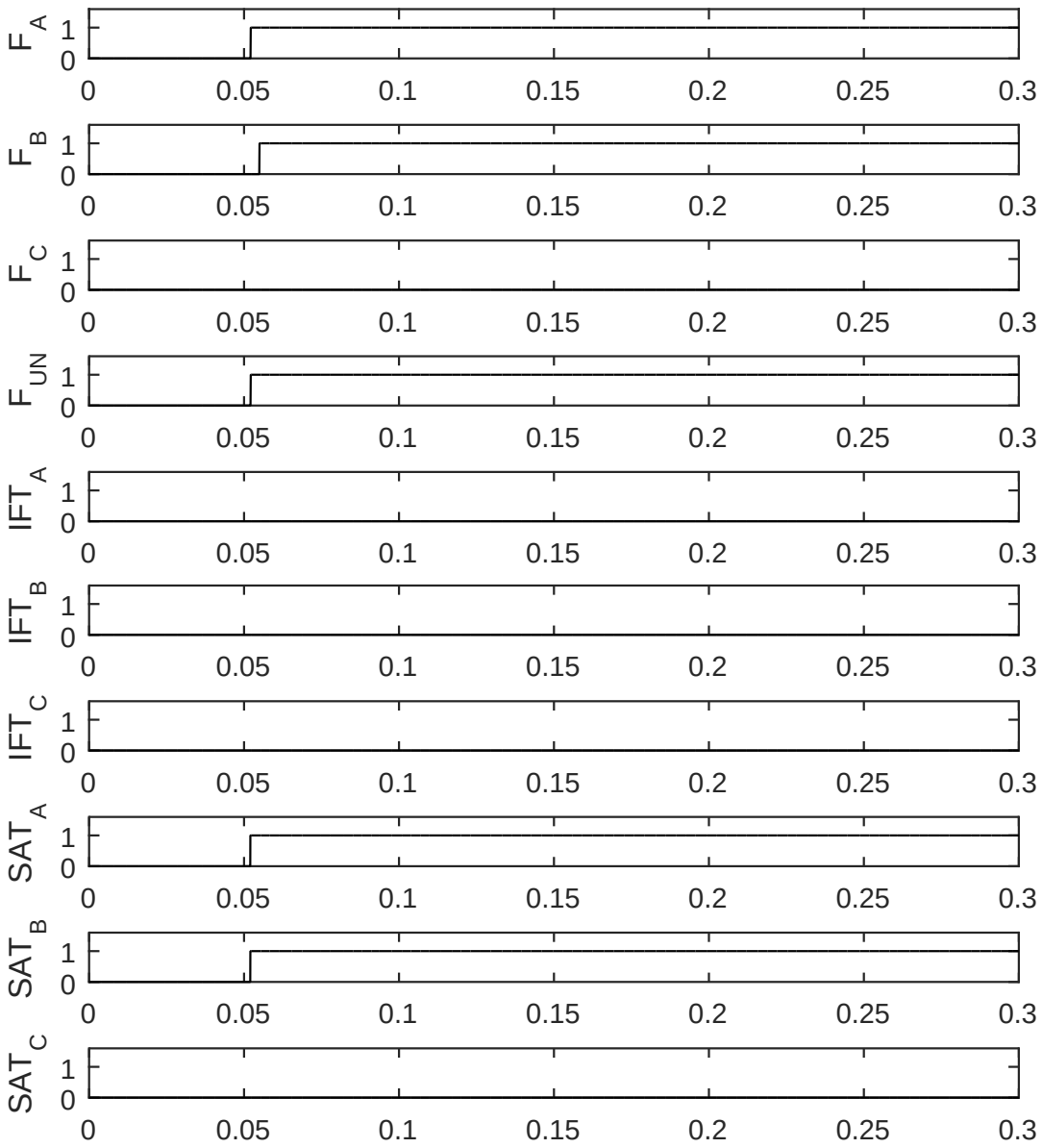

Figure 5.18: Response of proposed scheme for AB external fault with CT saturation part-(a)

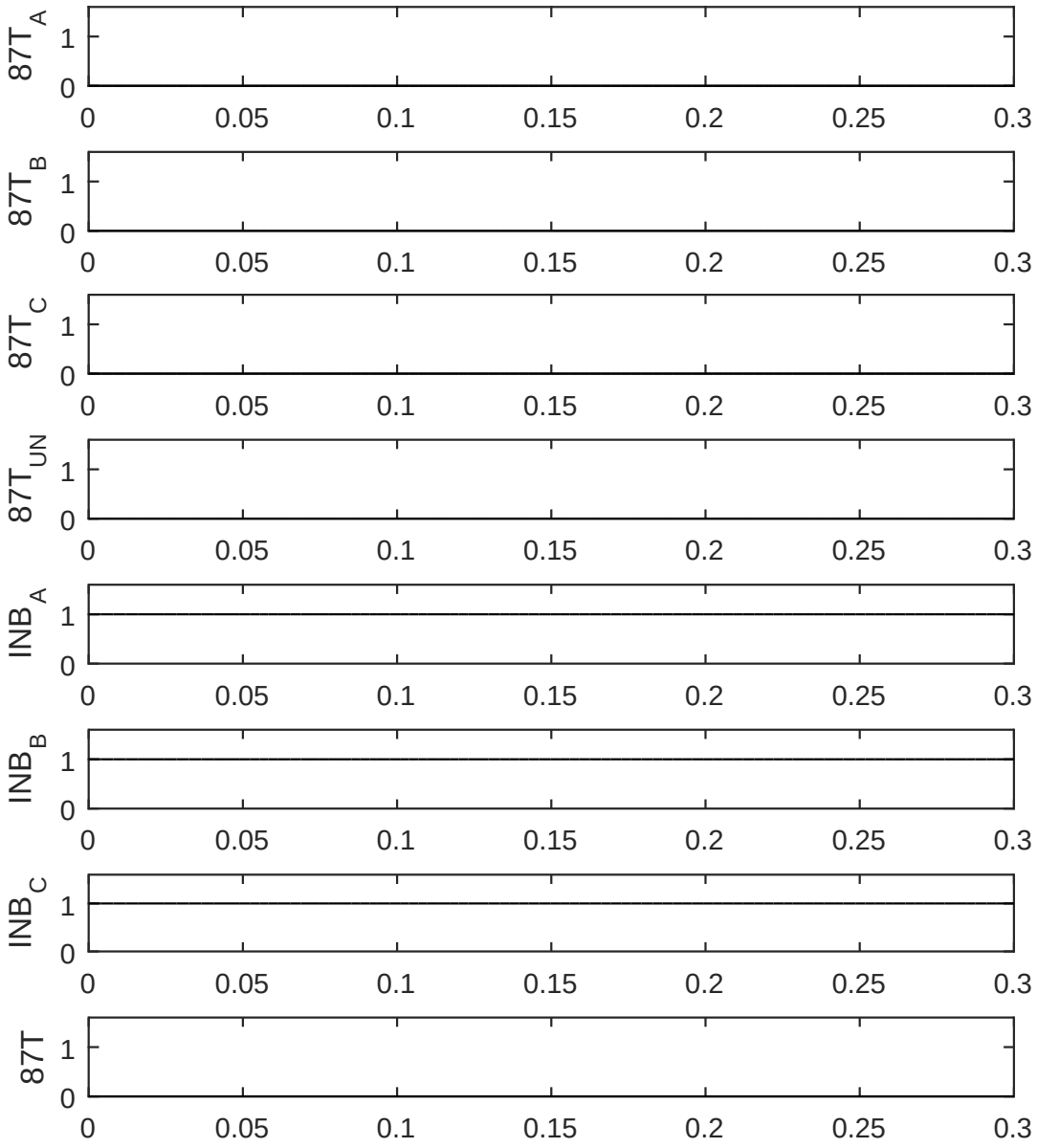

Figure 5.19: Response of proposed scheme for AB external fault with CT saturation part-(b)

Chapter 6

Line Differential Protection Scheme

Although, distance protection schemes with directional supervision are still widely used to protect transmission lines, current differential protection schemes are becoming popular with the deployment of advanced and high capapcity communication techniques. However, current differential protection has a major security concern during external faults under current transformer (CT) saturation. The existing line current differential phase element (87LP) designed for higher security suffers from lack of sensitivity. This paper proposes a new 87LP element based on partial operating current (POC) characteristics and time-domain CT saturation detection. The proposed 87LP element provides higher sensitivity for both symmetrical and asymmetrical internal faults without sacrificing security for external faults with CT saturation and therefore, eliminates the depndency on zero-sequence (87LG) and negative-sequence (87LQ) elements for higher sensitivity. The performance of the proposed 87LP element is evaluated in terms of security, sensitivity, dependability, and speed of operation by simulation study using Electro-Magnetic Transient Program (EMTP). The results are also compared with traditional 87LP element which works on alpha plane characteristics.

6.1 Scheme Design

The aim of the proposed scheme is to achieve higher sensitivity and faster relay operation in case of internal faults and at the same time maintain strong security for external faults or disturbances by using phase differential element. To achieve the targeted goal, the proposed line differential scheme uses the integrated logic of internal-external fault discriminator (IEF_p), phase fault detector (F_p), and CT saturation detector (SAT_p); where, p = A, B, C). The block diagram of the scheme is presented in Figure 6.1. Each element of the scheme is described in detail in the following subsections.

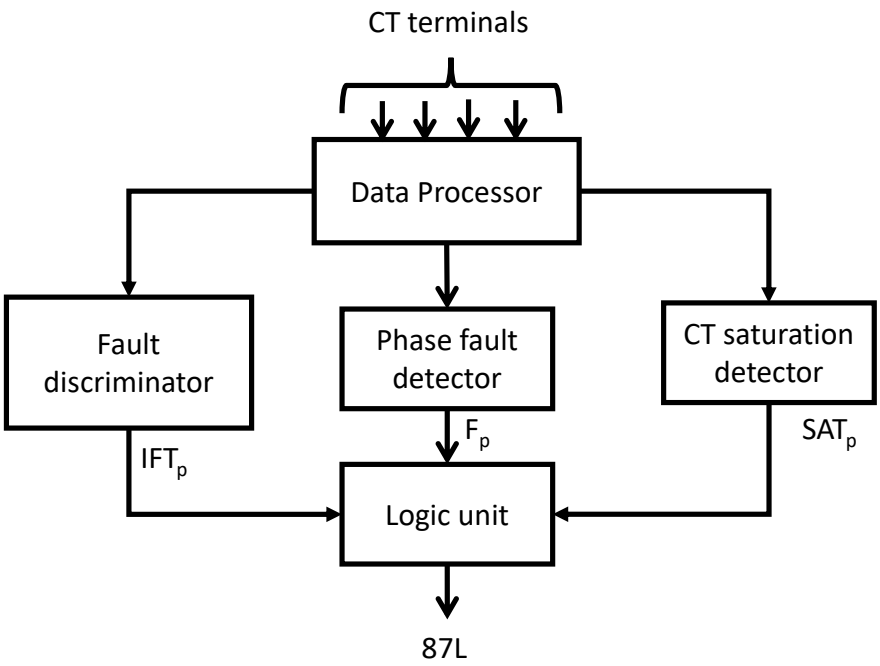

Figure 6.1: Basic block diagram of the proposed relay

6.1.1 Data Processor

The CT secondary currents are analog signals and they are sampled in a particular sampling rate to convert them into discrete signals. In this relay model, the sampling frequency is 200 samples per cycle. From these discrete signals, complex phasor values are extracted by using Discrete Fourier Transform (DFT) technique with a one cycle window as shown in Equation (6.1) [98].

$$I_{p_k} = \sum_{n=0}^{N-1} i_{p_k}(t_n) exp(-jwt_n) \tag{6.1}$$

In Equation (6.1): $i_{p_k}(t_n)$ is discrete current signal and I_{p_k} is the desired phasor of fundamental component. k, n, w, t_n and N represents terminal, sample number, angular frequency, time of n^{th} sample and sampling rate respectively.

6.1.2 Phase Fault Detector

The phase fault detection is an important element of the scheme because of their sensitivity to symmetrical faults. Phase differential element is designed based on single pickup (Ip_{pk}) setting irrespective of restraint current to detect the least amount of unexpected differential current. Slope characteristic is not considered as it reduces the sensitivity [27]. Pickup (Ip_{pk}) value is set as the maximum phase current mismatch resulted in from cumulative CT errors in the nominal system operating range. The output of the phase fault detector is denoted by F_p.

6.1.3 Fault Discriminator

The proposed internal-external fault discriminator works based on POC characteristics described in Section 3.3.2. POC algorithm calculates Partial Operating Currents (POCs) using cumulative vector addition of qualified terminal current phasors of the corresponding phase zone [74]. The qualified terminal current phasors $I_{p_1}, I_{p_2}, I_{p_3}, ..., I_{p_q}$ yield $(q-1)$ POCs as described in Equation (6.2) where, q indicates number of qualified terminals and p indicates corresponding phase (A, B, C).

$$I_{p_{op(k)}} = I_{p_{op(k-1)}} + I_{p_{k+1}} \tag{6.2}$$

In Equation (6.2): $k = 1, 2, ..., (q-1)$ with initial condition $I_{p_{op(0)}} = I_{p_1}$. $I_{p_{op(k-1)}}$ and $I_{p_{k+1}}$ represent two *input currents* of $I_{p_{op(k)}}$.

The POC characteristic presented in [74] shows that each resultant partial operating current for a protection zone is greater than the larger one of its two input currents during internal faults as described in Equation (6.3). However, for normal operation and external fault conditions irrespective of CT saturation, the statement of Equation (6.3) is violated. Equation (6.3) is a mathematical function to discriminate internal and external faults, which

eliminates the computational burden of phase angle measurement.

$$|I_{p_{op(k)}}| > max(|I_{p_{op(k-1)}}|, |I_{p_{k+1}}|) \quad for \;\; k = 1 : (q-1) \tag{6.3}$$

Equation (6.3) is referred to as "internal fault condition" and used in the design of the fault

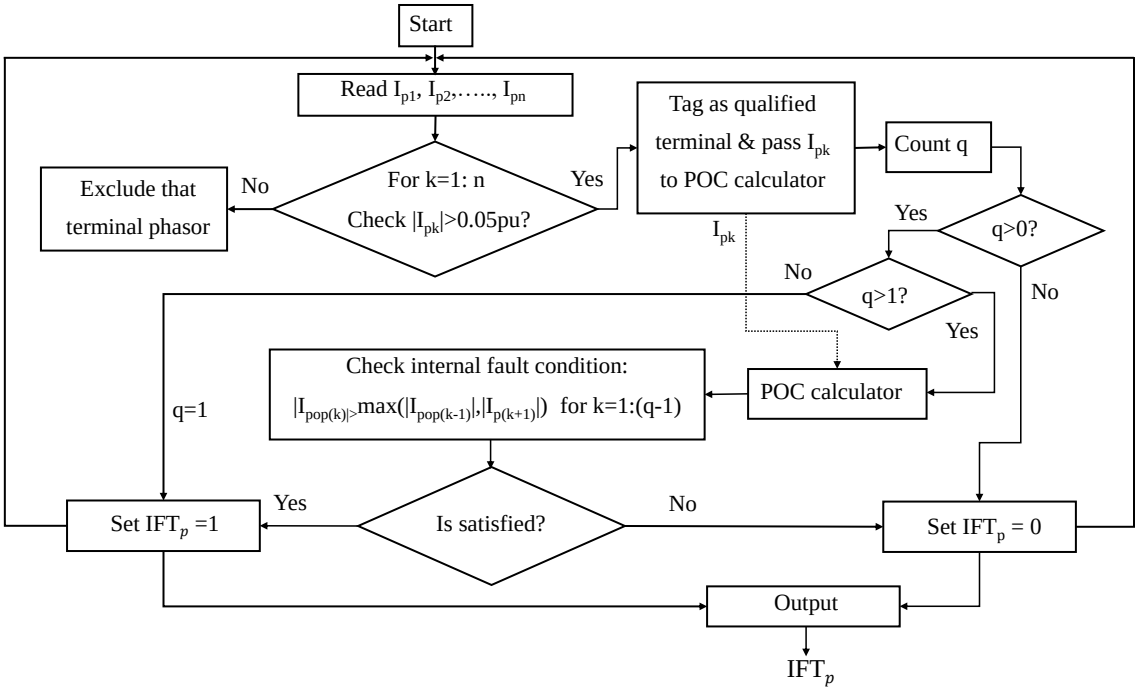

Figure 6.2: Flow chart of the POC algorithm

discriminator. The flow chart of fault discriminator algorithm is presented in Figure 6.2 and the output is denoted by IFT_p.

6.1.4 CT Saturation Detection

The proposed method to detect CT saturation during external faults which uses alienation coefficient of two instantaneous current signals found from the two-terminal equivalent model of the differential zone. The alienation coefficient is the indicator of non-similarity between two current signals [21] and during external faults alienation coefficient becomes high only in the event of CT saturation. CT does not saturate instantaneously with inception of

external faults. According to [95, 96], current waveforms remain undistorted at least for about 1/6 cycle before the first saturated waveform portion. The proposed method uses the time difference between fault inception and the starting of CT saturation. Alienation coefficient is used to determine the CT saturation starting time and fault inception time is calculated using first-derivative of the terminal currents. A generalized mathematical development for CT saturation detection is presented in Section 3.3.3. Figure 6.3 shows the proposed algorithm.

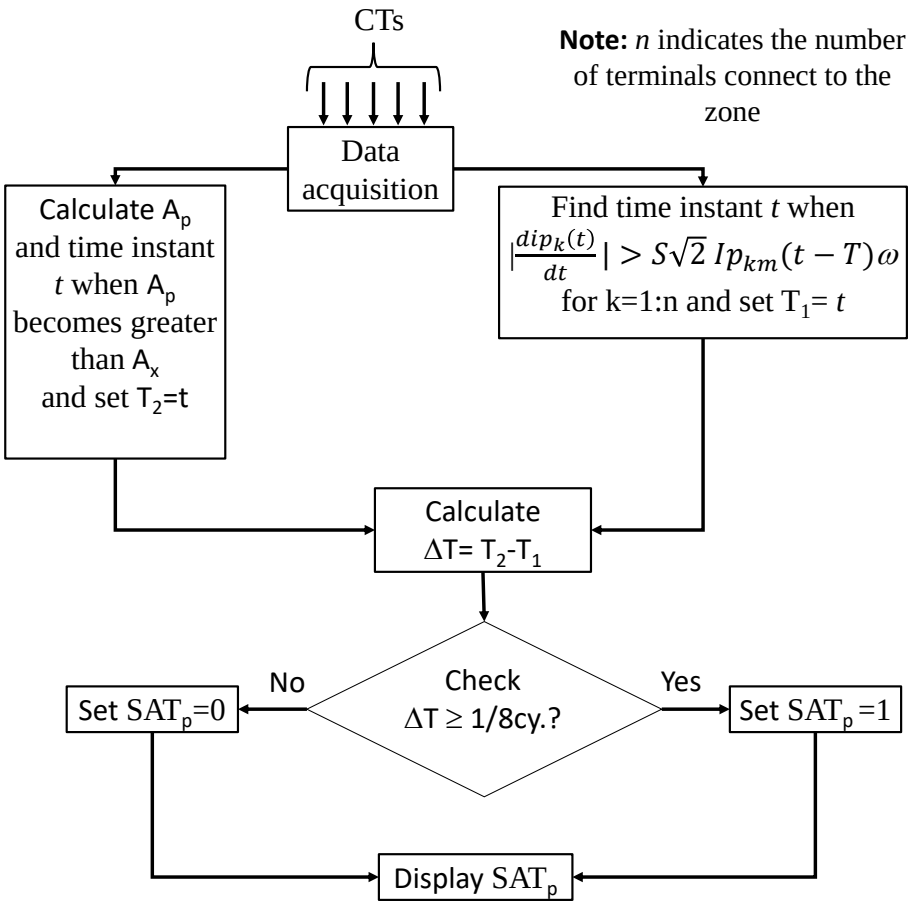

Figure 6.3: CT saturation detection algorithm

During internal bus faults, A_p becomes high instantaneously with the inception of faults [21]. However, A_p does not become high instantaneously with the inception of external faults. A_p is zero during external faults without CT saturation. Only the CT saturation event results in high value of A_p during external faults and CT saturation starts at least

1/6 cycle after the inception of faults [95, 96]. Therefore, A_p delays at least 1/6 cycle after fault inception to become high during external faults with CT saturation. The proposed CT saturation detection principle shown in Figure 6.3 considers a small processing time margin and declares CT saturation if the difference between fault inception time (T_1) and time instant (T_2) when A_p becomes high, is greater than or equal to 1/8 cycle or 2.04ms in 60Hz system. The time instant which satisfies the condition of Equation (3.45) for all terminal currents connected to the busbar, is the fault inception time (T_1). In this study, S is set to 2.0. T_2 is calculated by comparing A_p found from Equation (3.46) to a small positive set value A_x. In this study, A_x is set to 0.05 [21]. The output of the proposed CT saturation detector is denoted by SAT_p. SAT_p becomes high (logic 1) in the event of CT saturation during external faults.

6.1.5 Trip Logic Unit

Trip logic unit is the final block of the proposed differential relaying scheme. Trip logic unit decides whether to trip or block based on the outputs of fault detector unit (F_P), internal-external fault discriminator unit (IFT_P) and CT saturation detector unit (SAT_P), where P= A/B/C phase. Figure 6.4 shows the trip logic of the proposed scheme.

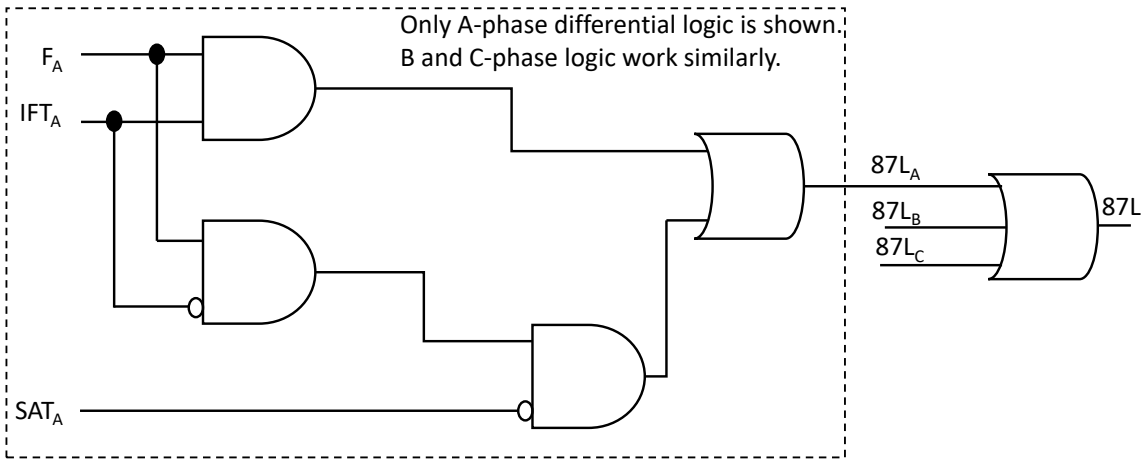

Figure 6.4: Trip logic

If both F_P and IFT_P are logic 1 for particular phase, the protected zone is definitely

encountered by an internal fault; therefore, the proposed protection scheme issues the trip signal without any delay.

When F_P is logic 1 and IFT_P is logic 0, the zone is under either external fault with CT saturation or high impedance internal fault. To discriminate the external fault with CT saturation from high impedance internal fault, a supervision technique based on CT saturation detection is used because during high impedance internal fault, fault current is low; therefore, CT remains unsaturated ($SAT_A = 0$). During high impedance internal faults, both IFT_P and SAT_P are logic 0 while F_P is logic 1 and the proposed scheme issues trip signal accordingly.

However, during external faults when CT saturation starts, F_P becomes logic 1 but IFT_P remains at logic 0 and saturation detection algorithm declares CT saturation ($SAT_P = 1$); therefore, the proposed differential scheme does not issue trip signal.

6.2 Testing

6.2.1 Test System and EMTP Model

The modified IEEE 14 bus test system shown in Figure 6.5 is used to test the performance of the proposed line differential protection scheme. The proposed scheme is applied in the line between bus 7 and 8 where the length of the line is 75 miles. The detail of the targeted line protection zone is shown in Figure 6.6. The test system parameters are presented in Appendix.

The above described test system is built in EMTP. In this study, constant-parameter distributed model is used to represent the transmission lines [99]. All generators are modeled as ideal sinusoidal voltage sources behind Thevenin impedances. The current transformers (CTs) are modeled by considering saturation impact. Figure 6.7 shows the CT model that is used in this study. This model represents an equivalent circuit built around an ideal transformer. CT parameters Rp, Lp, Ls, and inter-winding capacitance are very small which can be neglected [100]. In this study, inter-winding capacitance is neglected; however, Rp,

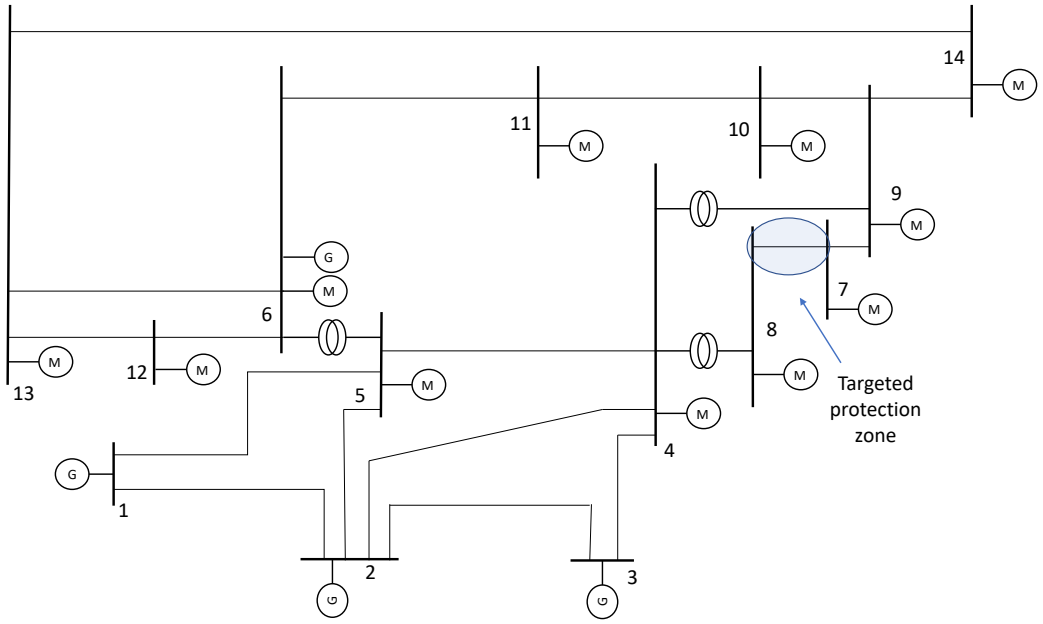

Figure 6.5: Modified IEEE 14 bus test system for Proposed Line Protection

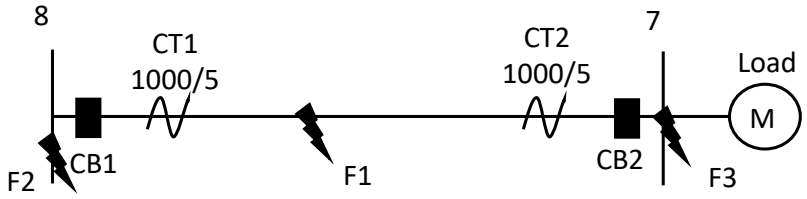

Figure 6.6: The detail of the targeted protection zone configuration

Lp, and Ls are taken into consideration. Rs represents combined CT secondary winding resistance, lead resistance, and the CT burden.

The magnetizing branch L_m is modeled as a nonlinear inductor element to include the effect of saturation [101]. The Φ-I characteristic of the non-linear inductor is adapted from [100].

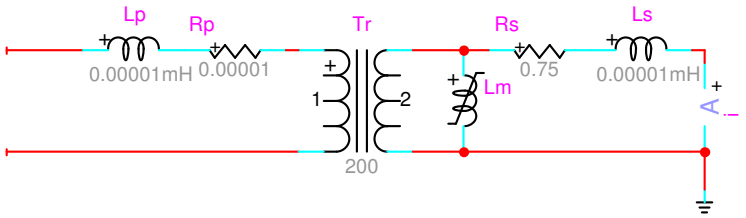

Figure 6.7: Line Protection: Current Transformer (CT) Model

6.2.2 Relay Model and Settings

The relay is modeled in Matlab platform based on the proposed relaying scheme described in Section 6.1. The performance of the fault detector depends on two setting values including phase pickup (Ip_{pk}), and load change tolerance (S). Table 6.1 shows the settings that are used in this study.

Table 6.1: Setting Values for the Proposed Line Protection Scheme

Ip_{pk} (pu)	S
0.1	1.2

6.2.3 Results and Discussions

As a power system element, a transmission line can be affected by any type of practical faults including Phase-Ground (PG), Phase-Phase (PP), Phase-Phase-Ground (PPG), Three-Phase (PPP) and Three-Phase-Ground (PPPG). To evaluate the performance of the proposed scheme, various tests were performed by applying faults in the EMTP model of the system shown in Figure 6.5 and Figure 6.6 at different locations (F_1, F_2 and F_3). The performed tests comprise various internal faults including phase-ground (PG), phase-phase (PP), phase-phase-ground (PPG) and three-phase (PPP, PPPG) and were simulated by varying fault resistance (R_f) to verify the sensitivity. All types of external faults were simulated in various CT saturation conditions by varying CT burden. The line between bus 7 and 9 was kept opened. The results of all test cases are documented in Table 6.3 and

compared with the existing alpha plane scheme [85]. The settings of alpha plane scheme are shown in Table 6.2.

Table 6.2: Setting Values for the alpha plane Scheme

Ip_{pk} (pu)	R	α (degree)
0.1	6	195

The results of the proposed scheme for three critical test cases which include PG internal fault for $R_f = 50$, PG internal fault for $R_f = 0.01$, and PP external fault are described below in detail.

6.2.3.1 Phase-Ground Internal Fault for $R_f = 50\Omega$

The waveforms shown in Figure 6.7 indicate a phase-ground (PG) internal fault which is applied to phase-A at $F1$. The fault is applied at t=0.05s where R_f is 50Ω. The current of phase-A at bus 8 side increases instantaneously with the inception of fault, where other two phases (B and C) are not affected. Due to high fault resistance, the current in phase-A remains almost same at bus 7 side. Figure 6.8 shows only F_A element is asserted at t=0.0526s because of high differential current and consequently, $87L_A$ and $87L$ elements are asserted at t=0.0526 as shown in Figure 6.9.

6.2.3.2 Phase-Ground Internal Fault for $R_f = 0.01\Omega$

The waveforms shown in Figure 6.10 indicate a phase-ground (PG) internal fault which is applied to phase-A at $F1$. The fault is applied at t=0.05s where R_f is 0.01Ω. The current of phase-A at bus 8 side increases instantaneously with the inception of fault, where other two phases (B and C) are not affected. Due to low fault resistance, the current in phase-A becomes zero almost same at bus 7 side. Figure 6.11 shows only F_A, and IFT_A elements are asserted at t=0.0515s and t=0.0588s, respectively and consequently, $87L_A$ and $87L$ elements are asserted at t=0.0515 as shown in Figure 6.12.

Table 6.3: Line Protection: Comparative analysis results

Fault	Location	Expected Result	R_f (Ω)	Burden (Ω)		Operating Time (ms)	
				CT1	CT2	Alpha Plane	PS
AG	F1	T	0.01	0.75	0.75	8.2	1.5
BC	F1	T	0.01	0.75	0.75	8.2	1.5
BCG	F1	T	0.01	0.75	0.75	8.2	1.5
ABC	F1	T	0.01	0.75	0.75	8.21	1.5
ABCG	F1	T	0.01	0.75	0.75	8.21	1.5
AG	F1	T	10	0.75	0.75	8.31	1.9
AG	F1	T	20	0.75	0.75	9.1	2.1
AG	F1	T	50	0.75	0.75	NT	2.6
AG	F1	T	100	0.75	0.75	NT	16.34
AG	F1	T	200	0.75	0.75	NT	16.66
AG	F2	NT	0.01	0.75	10	NT	NT
AG	F2	NT	0.01	0.75	25	NT	NT
AG	F2	NT	0.01	0.75	50	NT	NT
AG	F2	NT	0.01	0.75	100	NT	NT
AB	F2	NT	0.01	0.75	10	NT	NT
AB	F2	NT	0.01	0.75	25	NT	NT
AB	F2	NT	0.01	0.75	50	NT	NT
AB	F2	NT	0.01	0.75	100	NT	NT
BCG	F2	NT	0.01	0.75	10	NT	NT
BCG	F2	NT	0.01	0.75	25	NT	NT
BCG	F2	NT	0.01	0.75	50	NT	NT
BCG	F2	NT	0.01	0.75	100	NT	NT
ABC	F2	NT	0.01	0.75	10	NT	NT
ABC	F2	NT	0.01	0.75	25	NT	NT
ABC	F2	NT	0.01	0.75	50	NT	NT
ABC	F2	NT	0.01	0.75	100	NT	NT
ABCG	F2	NT	0.01	0.75	10	NT	NT
ABCG	F2	NT	0.01	0.75	25	NT	NT
ABCG	F2	NT	0.01	0.75	50	NT	NT
ABCG	F2	NT	0.01	0.75	100	NT	NT
AG	F3	NT	0.01	0.75	10	NT	NT
AG	F3	NT	0.01	0.75	25	NT	NT
AG	F3	NT	0.01	0.75	50	NT	NT
AG	F3	NT	0.01	0.75	100	NT	NT
AB	F3	NT	0.01	0.75	10	NT	NT
AB	F3	NT	0.01	0.75	25	NT	NT
AB	F3	NT	0.01	0.75	50	NT	NT
AB	F3	NT	0.01	0.75	100	NT	NT
BCG	F3	NT	0.01	0.75	10	NT	NT
BCG	F3	NT	0.01	0.75	25	NT	NT
BCG	F3	NT	0.01	0.75	50	NT	NT
BCG	F3	NT	0.01	0.75	100	NT	NT
ABC	F3	NT	0.01	0.75	10	NT	NT
ABC	F3	NT	0.01	0.75	25	NT	NT
ABC	F3	NT	0.01	0.75	50	NT	NT
ABC	F3	NT	0.01	0.75	100	NT	NT
ABCG	F3	NT	0.01	0.75	10	NT	NT
ABCG	F3	NT	0.01	0.75	25	NT	NT
ABCG	F3	NT	0.01	0.75	50	NT	NT
ABCG	F3	NT	0.01	0.75	100	NT	NT

Note:- T := Trip and NT:= No Trip

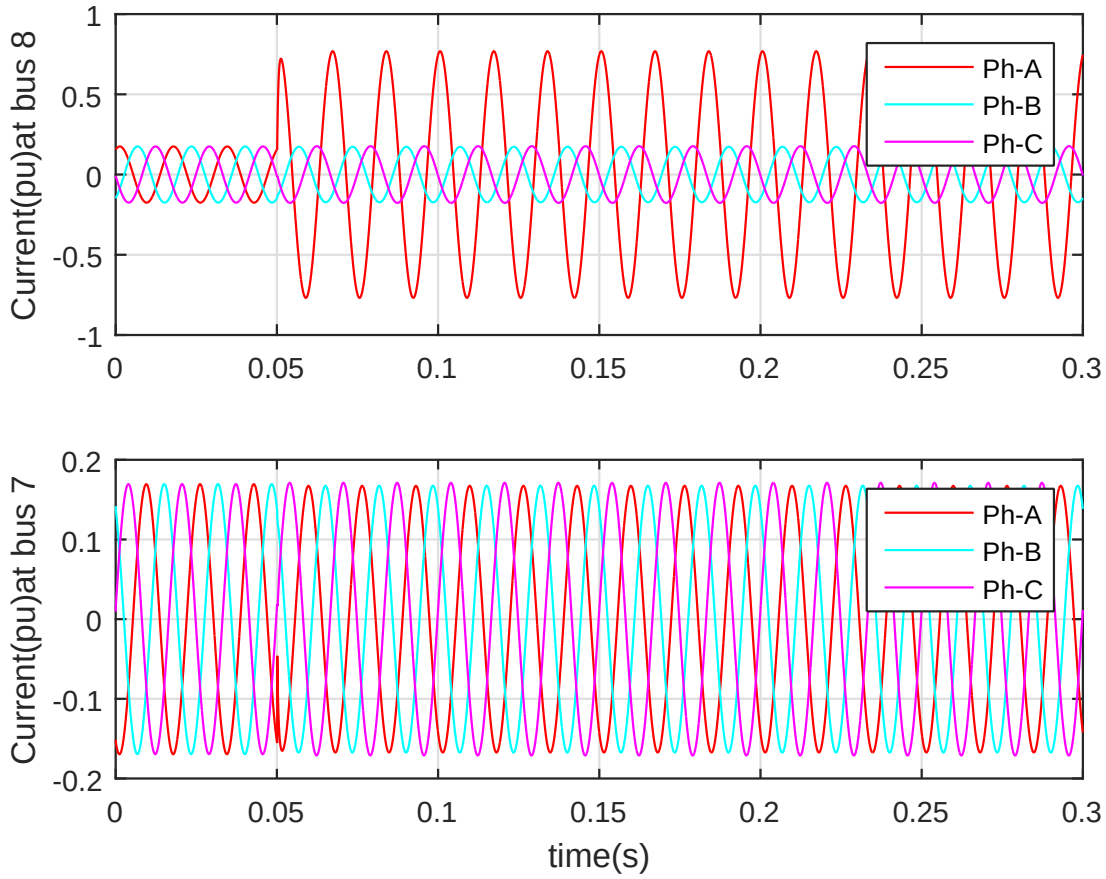

Figure 6.8: Fault currents waveforms during AG internal fault for $R_f = 50\Omega$

6.2.3.3 Phase-Phase external Fault

The waveforms shown in Figure 6.13 indicate a phase-phase (PP) external fault which is applied to phase A and B at $F3$. The fault is applied at t=0.05s. The current of phase A and B at bus 8 and at bus 7 side increase instantaneously with the inception of fault, where other phase (C) is not affected. Due to high fault currents. the CTs of phase-A and B at bus 7 side become saturated. F_A, and F_B elements are asserted because of high differential current resulted from CT saturation as shown in Figure 6.14. All fault discrimination are zero even after fault inception. All saturation elements except phase-C become high as soon as the CTs start saturation (at t=0.0526s). Therefore, all differential elements are zero even as expected as illustrated in Figure 6.15.

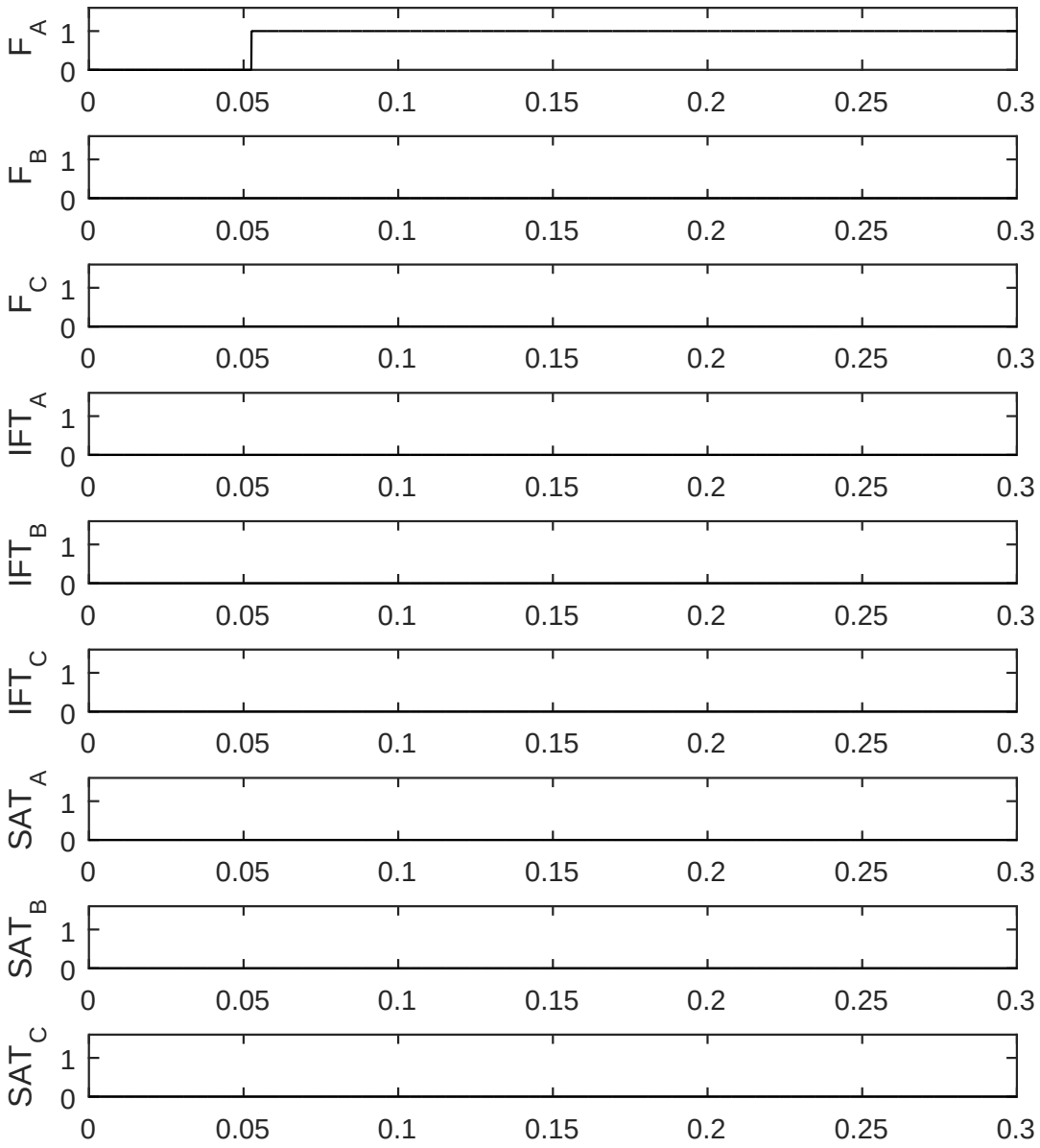

Figure 6.9: Response of proposed scheme for AG internal fault for $R_f = 50\Omega$- part (a)

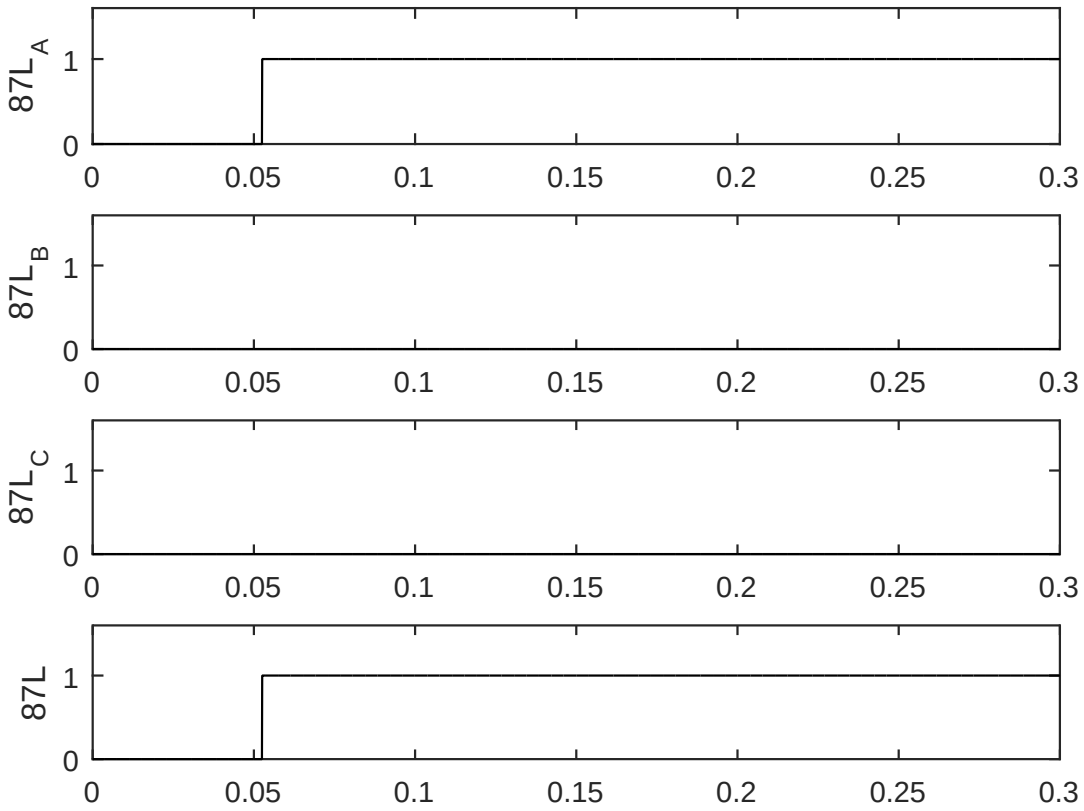

Figure 6.10: Response of proposed scheme for AG internal fault for $R_f = 50\Omega$- part (b)

6.2.3.4 Result Comparison

Table 6.3 shows the comparative performance of the proposed scheme (PS) with existing alpha plane scheme [85]. Both schemes perform expectedly during external faults with CT saturation. However, alpha plane scheme is unable to detect internal faults for cases where fault resistance is high and current inversion occurs. The proposed scheme (PS) performs as expected for all simulated faults irrespective of fault resistance and CT saturation conditions. The operating speed of the proposed scheme (PS) is faster than the alpha plane scheme.

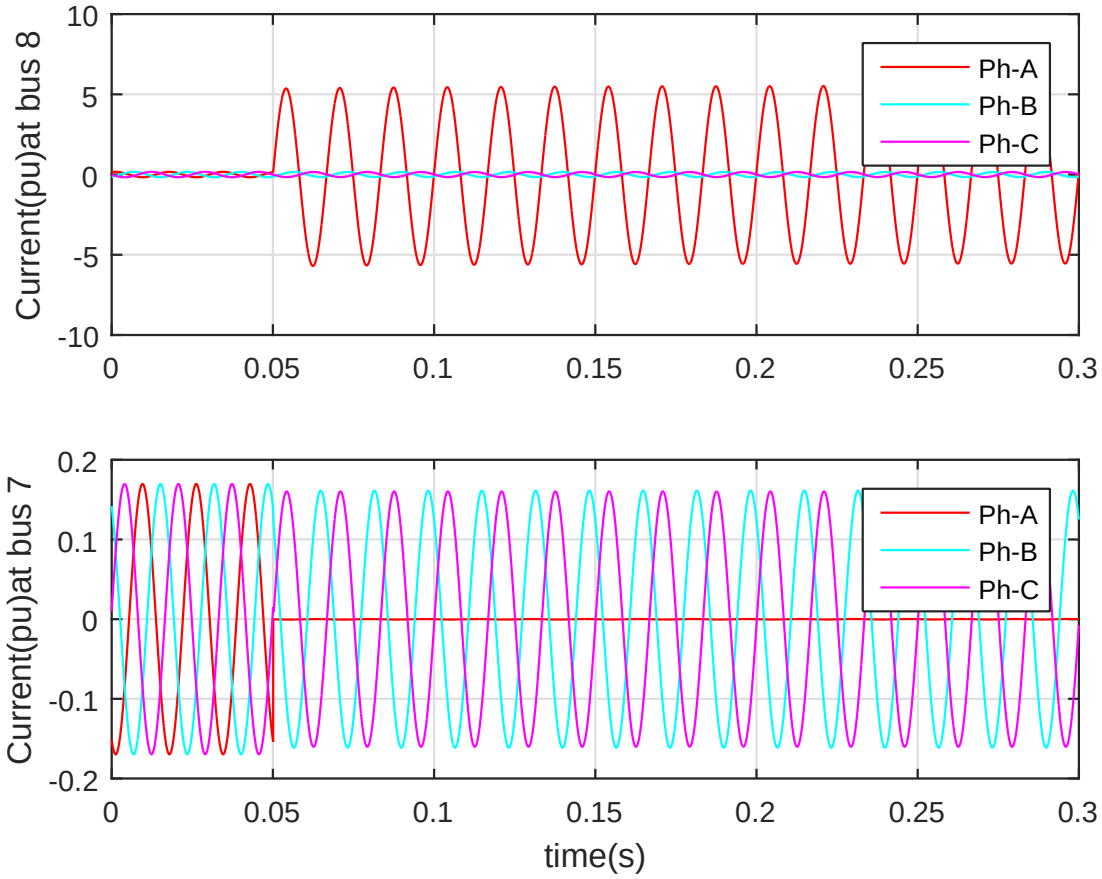

Figure 6.11: Fault currents waveforms during AG internal fault for $R_f = 0.01\Omega$

6.3 Summary

This chapter presents the scheme design as well as performance validation of the proposed line differential algrothim. The algorithm was tested for all possible fault scenarios which includes unusual scenarios such as CT saturation, fast CT saturation, high fault resistance, and DC offset. The results are also compared with the existing alpha plane scheme. Results documented in this chapter indicate that the proposed algorthm provides better security and sensitivity to transmission line for various fault conditions. The algorithm has not only overcome the CT saturation issues, it has also eliminated the concern of current inversion cases.

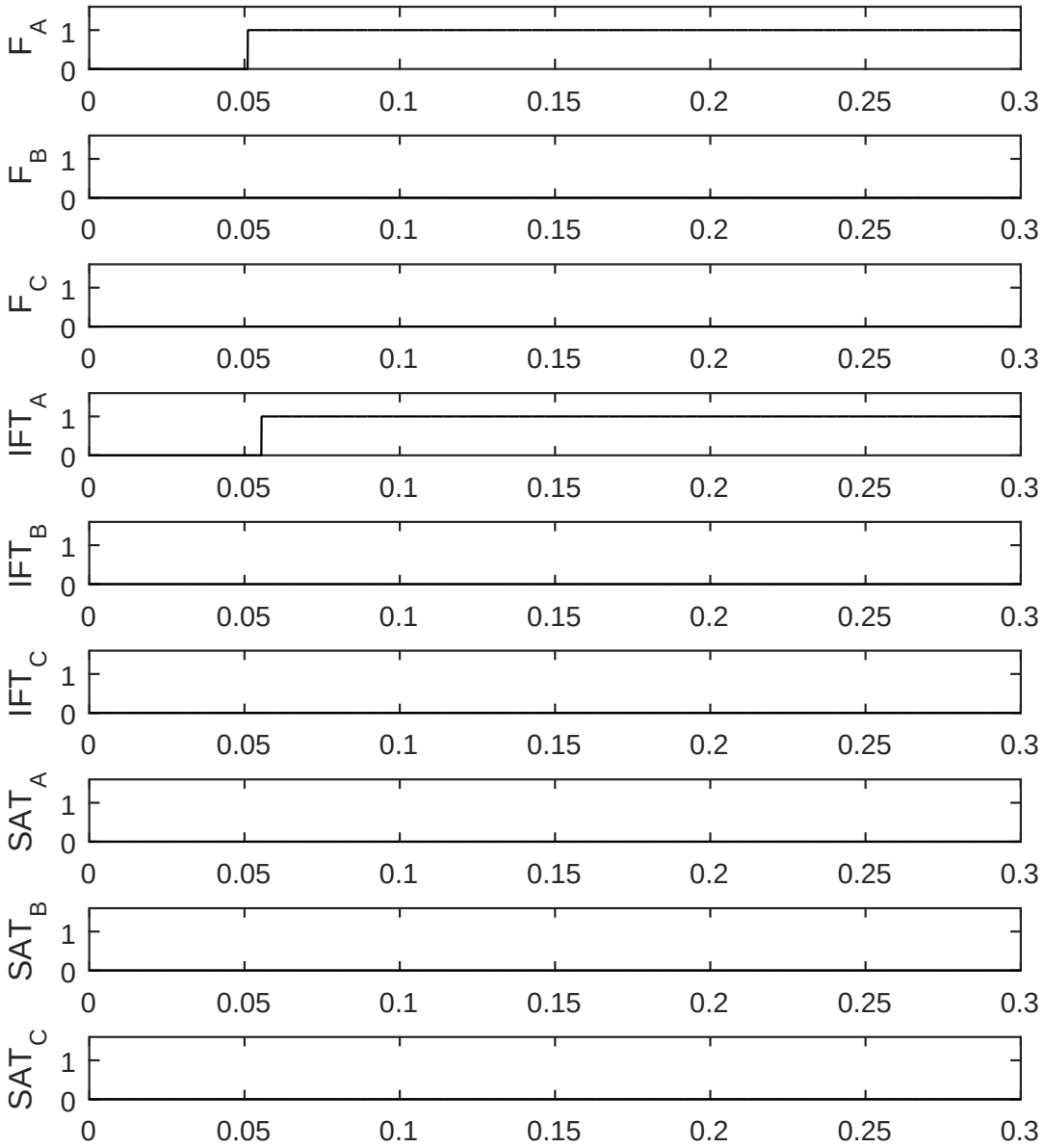

Figure 6.12: Response of proposed scheme for AG internal fault for $R_f = 0.01\Omega$- part (a)

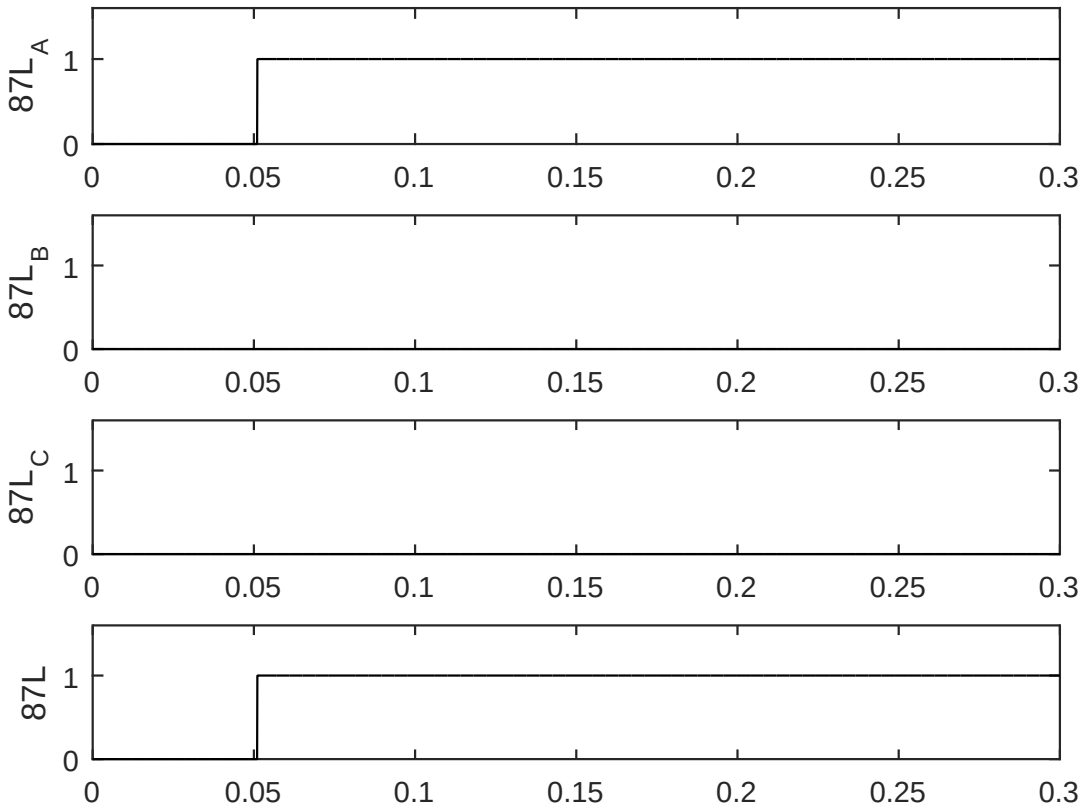

Figure 6.13: Response of proposed scheme for AG internal fault for $R_f = 0.01\Omega$- part (b)

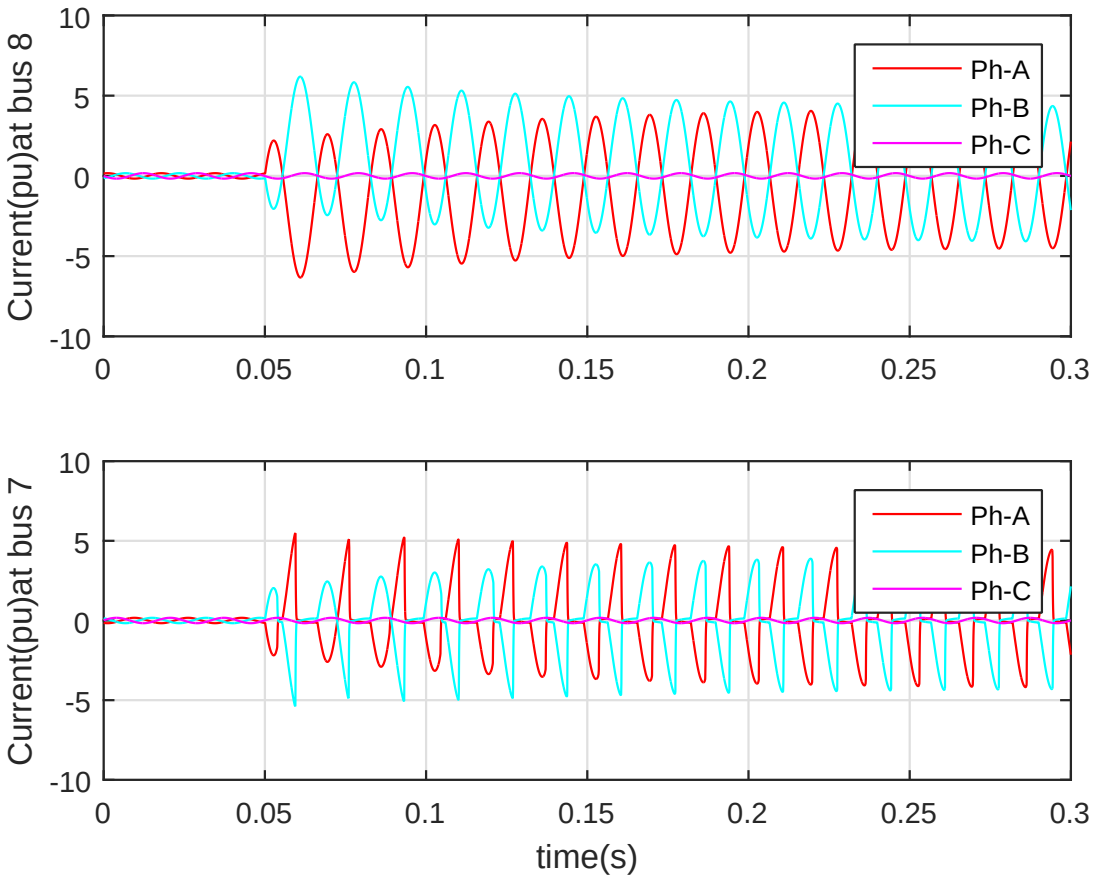

Figure 6.14: Fault currents waveforms during AB external fault with CT saturation

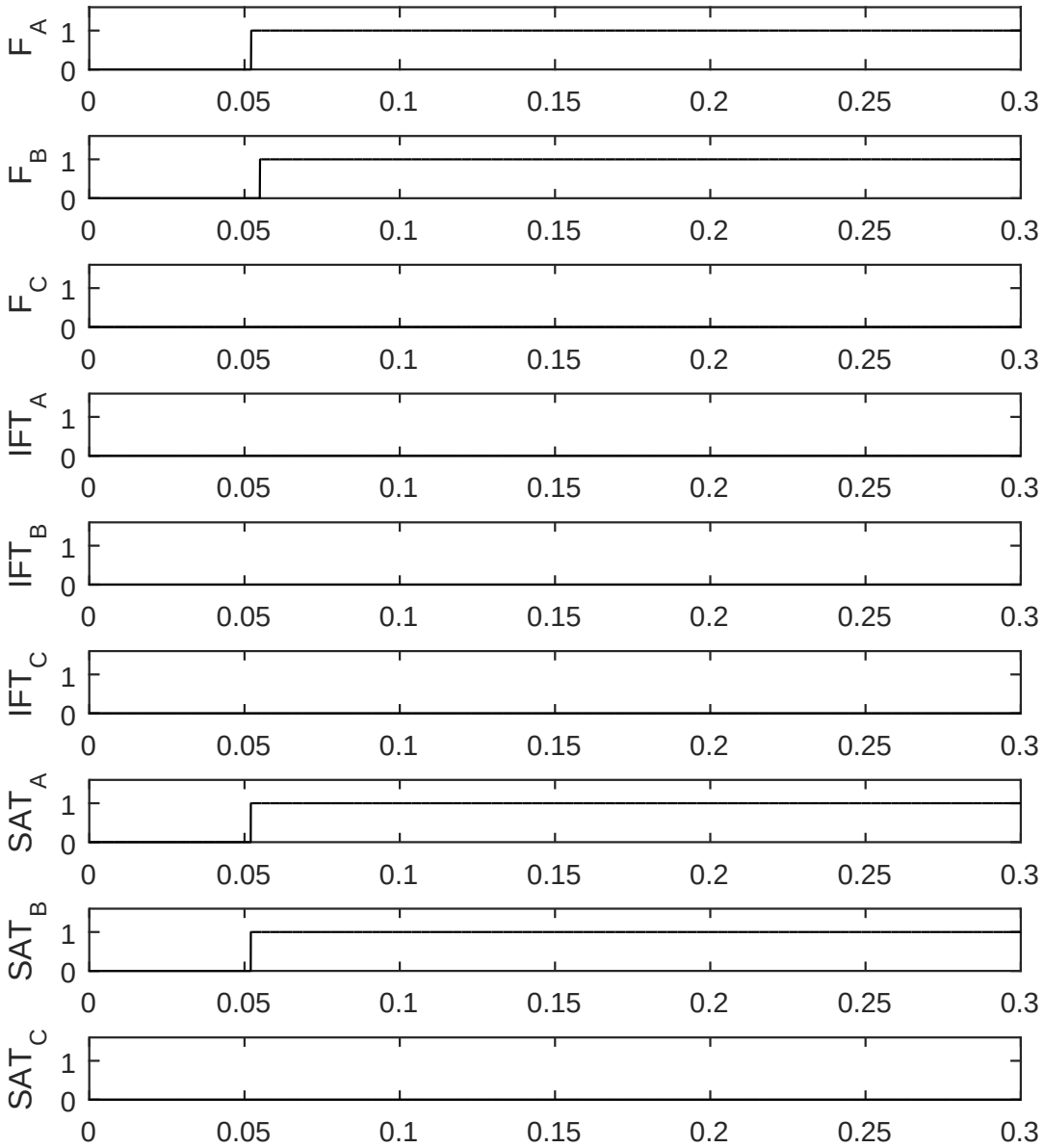

Figure 6.15: Response of proposed scheme for AB external fault with CT saturation part-(a)

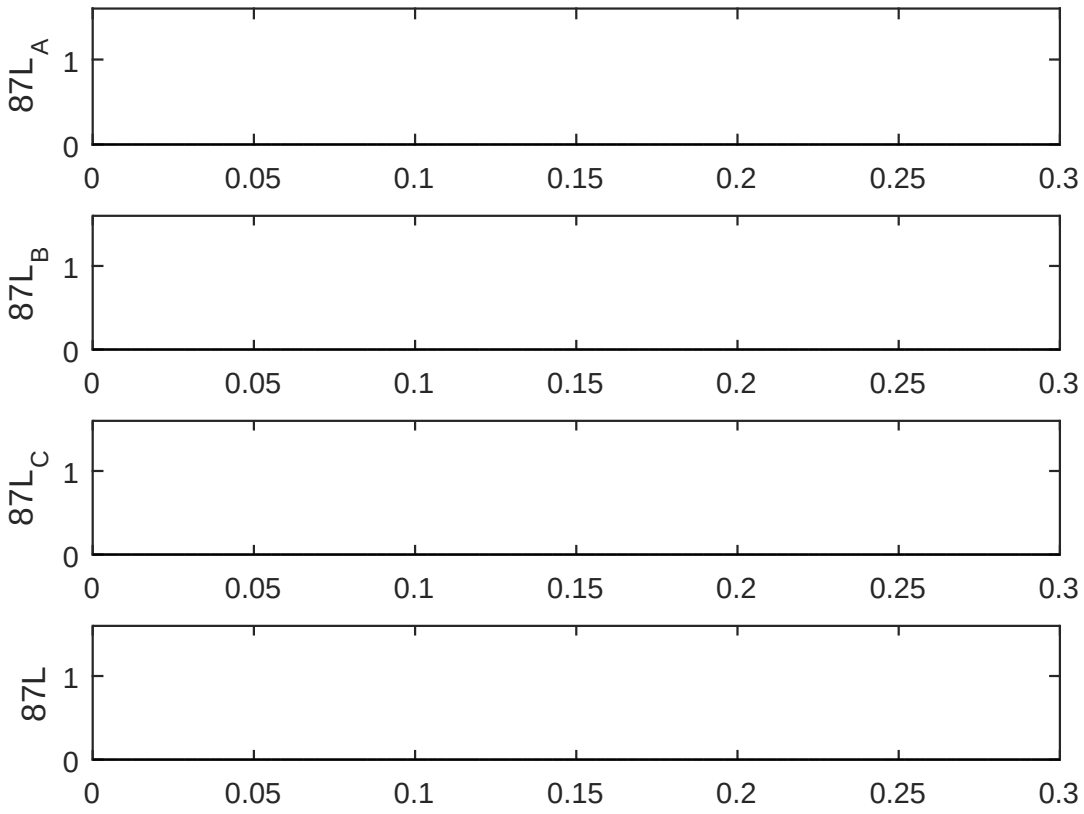

Figure 6.16: Response of proposed scheme for AB external fault with CT saturation part-(b)

Chapter 7

Concluding Remarks and Future Works

7.1 Concluding Remarks

This research work starts by exploring CT saturated current phasor characteristics. Based on the characteristics of CT saturated current phasor, the concept of Partial Operating Current (POC) characteristic is introduced. An analytical model of a time-domain CT saturation detection method is developed. This new CT saturation detection method and POC characteristic are used to discriminate the external and internal fault. The characteristics of the transformer inrush current waveform are explored to develop an inrush current blocking algorithm. Based on these new development, three separate differential schemes are designed for busbar, transformer, and line protection, respectively.

The proposed bus differential scheme uses partial operating current (POC) characteristics of a differential protection zone. To enhance the sensitivity of the proposed relaying scheme for very high impedance internal faults, a supervision technique based on newly developed CT saturation detection is incorporated. The relay model based on the proposed scheme is tested extensively using a transmission network simulated in EMTP for all possible faults under different practical scenarios such as fast CT saturation, slow CT saturation and high fault impedances. The proposed scheme is applied in a bus which is connected with active source and inactive source. The results of the simulation study show that the proposed scheme operates correctly for all internal faults irrespective of high or low impedance and blocks the trip during external faults even for severe CT saturation conditions. Overall, the proposed relaying scheme shows enhanced performance in terms of all four functional requirements of the power system protection including reliability, selectivity, sensitivity, and speed of operation.

The transformer differential scheme proposed in this dissertation has several enhanced

features. Firstly, the proposed scheme is very reliable and sensitive as it is capable of issuing the trip signal for all internal faults irrespective of fault resistance value. Secondly, the scheme provides strong security for fast as well as late CT saturation during external faults irrespective of CT saturation severity. Thirdly, the operating time of the scheme for any internal fault is smaller than or equal to 1 cycle which is very important for transformer protection as any delay in fault clearance can severely damage transformers. Fourthly, it is straightforward for relay engineers to configure the scheme because it has only few parameters to set. Finally, the proposed scheme has the less computational burden as it works on simple vector addition.

The existing line current differential phase element (87LP) designed for higher security suffers from lack of sensitivity. This dissertation presents a new 87LP element which uses POC characteristics and time-domain CT saturation detection. The proposed 87LP element provides higher sensitivity for both symmetrical and asymmetrical internal faults without sacrificing security for external faults with CT saturation and therefore, eliminates the depndency on zero-sequence (87LG) and negative-sequence (87LQ) elements for higher sensitivity. The performance of the proposed 87LP element was evaluated in terms of security, sensitivity, dependability, and speed of operation by simulation study using Electro-Magnetic Transient Program (EMTP). The results are also compared with traditional 87LP element which works on alpha plane characteristics. Results documented in this research indicate the capability of the proposed scheme to provide security to transmission line for various fault conditions. The algorithm has not only overcome the CT saturation issues, it has also eliminated the concern of current inversion cases.

7.2 Future Works

The differential schemes proposed in this dissertation are developed based on mathematical derivations. The algorithms are modelled in Matlab plateform and the performances are validated using simulated fault events in EMTP. In future, more research can be done on

this topic. The future research outlines are as follows:

1. Building prototypes of the proposed schemes.

2. Performance validation by Hardware-in-the-Loop (HIL) test.

3. Performance validation by using practical fault events recorded in DFRs. The collaboration with utility is required for this part of research.

Bibliography

[1] L. G. Hewitso, Mark Brown and Ramesh Balakrishna ,"Practical Power System Protection", Elsevier Ltd, 2005.

[2] The Electricity Training Association, "Power System Protection, Volumes 1-4", Institution of Engineering and Technology, 1995.

[3] Mason C. Russell, "Art and Science of Protective Relaying", John Wiley and Sons, New York, 1956.

[4] B. Chattopadhyay, M. S. Sachdev and T. S. Sidhu, "An on-line relay coordination algorithm for adaptive protection using linear programming technique", IEEE Trans. Power Delivery, vol. 11, no. 1, pp. 165 - 171, 1996.

[5] C. W. So and K. K. Li, "Time Coordination Method for Power System Protection by Evolutionary Algorithm", IEEE Industry Application, vol. 36, pp. 1235-1240, 2002.

[6] C. Martin, S. Chase and T. Nguyen, D. J. Hawaz and et al, "Bus Protection Considerations for Various Bus Types", 40th Annual Western Protective Relay Conference, 2013.

[7] Michael J. Thompson, "Percentage restrained differential percentage of what", 64th Annual Conference for Protective Relay Engineers, pp. 278-289, 2011.

[8] Ken Behrendt, David Costello and Stanley E. Zochol, "Considerations for Using High-Impedance or Low-Impedance Relays for Bus Differential Protection", 35th Annual Western Protective Relay Conference for Protective Relay Engineers, 2000.

[9] A. Guzman and et al, "Performance analysis betwwen traditional and improved transformer differential protection", 63rd Annual Conference for Protective Relay Engineers, pp. 1-16, 2009.

[10] Krish Narendra and Dave Fedirchuk, "Secured Busbar Differential Protection Using A Computationally Efficient Dot Product Technique", Power System Protection and Automation Conference, 2010.

[11] L.F. Kennedy and and C.D. Hayward, "Harmonic-current-restrained relays for differential protection", AIEE transaction, vol. 57, no. 5, pp. 262-266, 1938.

[12] A.G. Phadke and J.S. Thorp, "Computer relaying for power systems", Research Studies Press LTD., 1988.

[13] J.B. Royle and A. Hill, "Low impedance biased differential busbar protection for application to busbars of widely differing configuration", IEE 4th Int. Conf. on Developments in Power System Protection, pp. 40-44, 1989.

[14] F. Andow, Y. Murakamy and K. Inamural, "Microprocessor-based busbar protection relay", IEE 5th Int. Conf. on Developments in Power System Protection, pp. 103-106, 1993.

[15] C. Fernandez, "An Impedance-based CT saturation detection algorithm for bus-bar differential protection", IEEE Transactions of Power Delivery, vol. 16, no. 4, pp. 468-472, 2001.

[16] H. S. Gill, T. S. Sidhu and Ms. S. Sachdev, "Microprocessor-based busbar protection system", IEEE Transactions of Power Delivery, vol. 147, no. 4, pp. 252-260, 2002.

[17] S.H. Horowitz and A.G. Phadke, "Power system relaying", Research Studies Press LTD., 1992.

[18] Yong-Cheol Kang, Ui-Jai Lim, Sang-Hee Kang and Peter A. Crossley, "A busbar differential protection relay suitable for use with measurement type current transformers", IEEE Transactions of Power Delivery, vol. 20, no. 2, pp. 1291-1298, 2005.

[19] Shaik Abul Gafoor, N. Rama Devi and P. V. Ramana Rao, "A transient current based bus zone protection scheme using wavelet transform", ICSET, pp. 1195-1199, 2008.

[20] K. Narendra, D. Fedirchuk, N. Zhang, R. Midence, N. Perera and V. Sood, "Phase angle comparison and differential rate of change methods used for differential protection of busbars and transformers", IEEE Electrical Power and Energy Conference, pp. 134-139, 2011.

[21] R. Abd Allah, "Busbar protection scheme based on alienation coefficients for current signals", IJEAT, vol. 3, pp. 103-115, 2014.

[22] R. Abd Allah, "Experimental results and technique evaluation based on alienation coefficients for busbar protection scheme", Elsevier, Int. J. Electr. Power Energy Syst., vol. 73, pp. 943-954, 2015.

[23] R. Abd Allah, "Adaptive busbar differential relaying scheme during saturation period of current transformers based on alienation concept", IET Generation, Transmission and Distribution., vol. 10, no. 15, pp. 3803-3815, 2016.

[24] Hamed Dashti and Majid Sanaye Pasand, "Power transformer protection using a multiregion adaptive differential relay", IEEE Trans. Power Deliv., vol. 53, no. 3, pp. 2642-2649, 2017.

[25] A. Guzman, N. Fischer and C. Labuschagne, "Improvements intransformer protection and control", 62nd Protect. Relay Eng. Annu. Conf.e, pp. 563-579, 2009.

[26] W. Schossig, "Introduction to the history of differential protection", PAC World Mag., 2008.

[27] M. Stanbury and Zarko Djekic, "The impact of current transformer saturation on transformer differential protection", IEEE Trans. Power Deliv., vol. 30, no. 3, pp. 1278-1287, 2015.

[28] Lubomir Sevov, Umar Khan and Zhiying Zhang, "Enhancing Power Transformer Differential Protection to Improve Security and Dependability", IEEE Transactions on Industry Applications, vol. 47, no. 2, pp. 1003-1012, 2011.

[29] Abdolaziz Ashrafian, Mojtaba Mirsalim and Mohammad A. S. Masoum, "Application of a Recursive Phasor Estimation Method for Adaptive Fault Component Based Differential Protection of Power Transformers", IEEE Transactions on Industrial Informatics, vol. 13, no. 3, pp. 1381-1392, 2017.

[30] B. Kasztenny, G. Brunello and L. Sevov, "Digital low impedance bus differential protection with reduced requirements for CTss", IEEE Transmission and distribution conference and exposition, pp. 703-708, 2001.

[31] K. Narendra, D. Fedirchuk and N. Zhang, "Differential rate of change method for busbar protection", US Patent 20120182657A1, 2012.

[32] E.C. Segatto and D.V. Coury, "A differential relay for power transformers using intelligent tools", IEEE Transactions on Industrial Informatics, vol. 21, no. 3, pp. 1154-1162, 2006.

[33] M. Tripathy, R.P. Maheshwari and H.K. Verma, "Probabilistic neural-network-based protection of power transformers", IET Electric Power Applications, vol. 1, no. 5, pp. 793-798, 2007.

[34] M. Tripathy, R.P. Maheshwari and H.K. Verma, "Power Transformer Differential Protection Based On Optimal Probabilistic Neural Network", IEEE Trans. Power Deliv., vol. 25, no. 1, pp. 102-112, 2010.

[35] Myong-Chul Shin, Chul-Won Park and Jong-Hyung Kim, "Fuzzy logic-based relaying for large power transformer protection", IEEE Trans. Power Deliv., vol. 18, no. 3, pp. 718-714, 2003.

[36] Daniel Barbosa, Ulisses Chemin Netto, Denis V. Coury and Mário Oleskovicz, "Power Transformer Differential Protection Based on Clarke's Transform and Fuzzy Systems", IEEE Trans. Power Deliv., vol. 26, no. 2, pp. 1212-1220, 2011.

[37] Daniel Barbosa, Denis V. Coury and Mário Oleskovicz, "New approach for power transformer protection based on intelligent hybrid systems", IET Generation Transmission and Distribution, vol. 6, no. 10, pp. 1009-1018, 2012.

[38] S. A. Saleh and M. A. Rahman, "Modeling and protection of a three-phase power transformer using wavelet packet transform", IEEE Trans. Power Deliv., vol. 20, no. 2, pp. 1273-1282, 2005.

[39] S. A. Saleh, Benjamin Scaplen and M. A. Rahman, "A New Implementation Method of Wavelet-Packet-Transform Differential Protection for Power Transformers", IEEE Transactions on Industry Applications, vol. 47, no. 2, pp. 1003-1012, 2011.

[40] S. A. Saleh, A. Aktaibi, R. Ahshan and M. A. Rahman, "The Development of a d– q Axis WPT-Based Digital Protection for Power Transformers", IEEE Trans. Power Deliv., vol. 27, no. 4, pp. 2255-2269, 2012.

[41] R. P. Medeiros, F. B. Costa and K. M. Silva, "Power Transformer Differential Protection Using the Boundary Discrete Wavelet Transform", IEEE Trans. Power Deliv., vol. 31, no. 5, pp. 2083-2095, 2016.

[42] Senthil Kumar Murugan, Sishaj P Simon, Kinattingal and et al, "An Empirical Fourier Transform-Based Power Transformer Differential Protection", IEEE Trans. Power Deliv., vol. 32, no. 1, pp. 209-218, 2017.

[43] S. C. Sun and R. E. Ray, "A current differential relay systems using fiber optics communications", IEEE Trans. Power Appar. Syst., vol. 102, no. 2, pp. 410-419, 1983.

[44] J. D. Huddleston and T. A. Phillippe, "A survey of optical channels for protective relaying practices and experience", IEEE Trans. Power Deliv., vol. 10, no. 2, pp. 647-658, 1995.

[45] H. Y. Li, E. P Southern and et a, "A new type of differential feeder protection relay using global positioning system for data synchronization", IEEE Trans. Power Deliv., vol. 12, no. 3, pp. 1090-1099, 1997.

[46] A. R. C. Warrington, "Protective relays: Their theory and applications", Chapman and Hall, 1962.

[47] IEEE PSRC Report, "Line protection design trends in the USA and Canada", IEEE Trans. Power Deliv., vol. 3, no. 4, pp. 1530-1535, 1988.

[48] Z. Y. Xu, Z. Q. Du and L. Ran and et al, "A current differential relay for a 1000KV UHV transmission line", IEEE Trans. Power Deliv., vol. 22, no. 3, pp. 1177-1182, 2007.

[49] Hank Miller, John Burger and et al, "Modern line current differential protection solutions", 36th Annual Western Protective Relay Conference, 2009.

[50] M.E. Masoud and M.M.A. Mahfouz, "Protection scheme for transmission lines based on alienation coefficients for current signals", IET Generation, Transmission and Distribution, vol. 4, no. 11, pp. 1236-1240, 2010.

[51] K. M. Silva and R. G. Bainy, "Generalized Alpha Plane for Numerical Differential Protection Applications", IEEE Trans. Power Deliv., vol. 31, no. 6, pp. 2566-2566, 2016.

[52] Y. Xue, B. Kasztenny, D. Taylor and et al, "Line differential protection under unusual system conditions", 67th Annual Georgia Tech Protective relaying Conference, 2013.

[53] G. Benmouyal and T. Lee, "Securing sequence current differential elements", 31st Annual Western Protective relaying Conference, 2004.

[54] Sanjay Dambhare, S. A. Soman and M. C. Chandorkar, "Adaptive Current Differential Protection Schemes for Transmission Line Protection", IEEE Trans. Power Deliv., vol. 24, no. 4, pp. 1832-1841, 2009.

[55] Shihong Miao, Pei Liu and Xiangning Lin, "An Adaptive Operating Characteristic to Improve the Operation Stability of Percentage Differential Protection", IEEE Trans. Power Deliv., vol. 25, no. 3, pp. 1410-1417, 2010.

[56] Maria Leonor, S. Almeida and Kleber M. Silva, "Transmission lines differential protection based on an alternative incremental complex power alpha plane", IET Generation, Transmission and Distribution, vol. 11, no. 1, pp. 10-17, 2017.

[57] Saumendra Sarangi and Ashok Kumar Pradhan, "Adaptive alpha plane line differential protectione", IET Generation, Transmission and Distribution, vol. 11, no. 10, pp. 2468-2477, 2017.

[58] J. Roberts, D. Tziouvaras, G. Benmouyal. and et al, "The effect of multiprinciple line protection on dependability and security", Southern African Power System Protection Conferencee, 2000.

[59] "Transient response of current transformers", IEEE Transactions on Power Apparatus and Systems, vol. 96, no. 6, pp. 1809-1814, 1977.

[60] Ionuţ Ciprian BORĂSCU, "The CT Behavior and Its Compatibility with Relay Protection", U.P.B. Sci. Bull, 2014.

[61] A. Writght and C. Christopoulos, "Electrical Power System Protection", Chapman and Hall , 1993.

[62] Y. C. Kang, J. K. Park, S. H. Kang, A. T. Johns and R. K. Aggarwal, "An algorithm for compensating the secondary current of current transformers", IEEE Trans. Power Deliv., vol. 12, pp. 116-124, 1997.

[63] T. Bunyagu, P. Crossley and P. Gale, "Overcurrent protection using signals derived from saturated measurement CTs", Proc. IEEE Power Eng. Soc. Summer Meeting, 2001.

[64] Y. C. Kang, S. H. Ok and S. H. Kang, "A CT saturation detection algorithm", IEEE Trans. Power Deliv., vol. 19, pp. 78-85, 2004.

[65] Nicholas Villamagna and Peter A. Crossley, "A CT Saturation Detection Algorithm Using Symmetrical Components for Current Differential Protection", IEEE Trans. Power Deliv., vol. 21, no. 1, 2006.

[66] Zhiying Zhang, Krish Narendra, Dave Fedirchuk, George Punnoose and Premnath, "A Novel CT Saturation Detection Algorithm for Bus Differential Protection".

[67] Dave Fedirchuk, "Electrical Bus Protection Method and Apparatus", US Patent - 7199991 B2, 2007.

[68] Randy Hamilton, "Analysis of transformer inrush current and comparison of harmonic restraint methods in transformer protection", IEEE Trans. on Industrial Applications, vol. 49, no. 4, pp. 1890-1899, 2013.

[69] R. Patterson, W. McCannon and G. Kobet, "A consideration of inrush restaint methods in transformer differential relays", 54th Annual Georgia Tech. Protection Relay Conference, 2000.

[70] L. Lawhead and R. Hamilton, "Harmonic sharing for effective detection of transformer inrush condition in differential protection schemes", 31st Annual Western. Protection Relay Conference, 2004.

[71] B. Kasztenny and A. Kulidjian, "An improved transformer inrush restraint algorithm increases security while maintaining fault response performance", 53rd Annual Western. Protection Relay Conference, 2000.

[72] R. Hunt, J. Schaefer and B. Bentert, "Practical experience in setting transformer differential inrush restraint", 61st Annual Georgia Tech. Protection Relay Conference, 2007.

[73] Monir Hossain, "Fault Discrimination Algorithm for Busbar Differential Protection Relaying Using Partial Operating Current Characteristics", University of New Orleans Theses and Dissertations, 2016.

[74] Monir Hossain, Ittiphong Leevongwat and Parviz Rastgoufard, "Partial operating current characteristics to discriminate internal and external faults of differential protection zones during CT saturation", IET Generation, Transmission and Distribution, vol. 12, no. 2, pp. 379-387, 2018.

[75] Monir Hossain, Ittiphong Leevongwat and Parviz Rastgoufard, "Design and testing of a bus differential protection scheme using partial operating current (POC) algorithm", Electric Power Systems Research, vol. 157, pp. 29-38, 2018.

[76] Monir Hossain, Ittiphong Leevongwat and Parviz Rastgoufard, "Revisions on Alpha Plane for Enhanced Sensitivity of Line Differential Protection", Electric Power Systems Research, Early Access Article, 2018.

[77] Monir Hossain, Ittiphong Leevongwat and Parviz Rastgoufard, "Comparative analysis of fault discrimination algorithms on sensitivity to high impedance busbar faults", North American Power Symposium (NAPS), pp. 1-6, 2017.

[78] Monir Hossain, Lipika Mittal and Parviz Rastgoufard, "A dynamic current allocation algorithm for alienation coefficient based busbar fault discriminator", 19th International Conference on Intelligent System Application to Power Systems (ISAP), pp. 1-6, 2017.

[79] Monir Hossain, Ittiphong Leevongwat and Parviz Rastgoufard, "Fast fault detection challenge for alienation coefficient based bus fault discriminaton", 71st Annual Conference for Protective Relay Engineers (CPRE), pp. 1-6, 2018.

[80] Monir Hossain, Ittiphong Leevongwat and Parviz Rastgoufard, "A CT saturation detection method for bus differential protection", Clemson power systems conference, 2018.

[81] Monir Hossain, Ittiphong Leevongwat and Parviz Rastgoufard, "Enhanced transformer differential protection", Under preparation.

[82] Monir Hossain, Ittiphong Leevongwat and Parviz Rastgoufard, "Line differential protection using POC", Under preparation.

[83] Clayton R. Paul, "Fundamentals of Electric Circuit Analysis", John Wiley and Sons, 2001.

[84] Q.H. Wu, Zhen Lu and Tianyao Jil, "Protective Relaying of Power Systems Using Mathematical Morphology", Springer, 2009.

[85] SEL-311L-1, -7 Relay, Instruction Manual, SEL Inc., Pullman, Washington, 2016.

[86] D. A. Tziouvaras and et al, "Mathematical Models for Current, Voltage, and Coupling Capacitor Voltage Transformers", IEEE Transactions on Power Delivery, pp. 62-72, 2000.

[87] Fawwaz T. Ulabyi, "Fundamentals of Applied Electromagnetics", Prentice Hall, 2007.

[88] M. Jamali, M. Mirzaie and S. Asghar-Gholamian, "Calculation and Analysis of Transformer Inrush Current Based on Parameters of Transformer and Operating Conditions", Electronics and Electrical Engineering, vol. 109, pp. 17-20, 2011.

[89] K. W. Sonnemann, C. L. Wagner and G. D. Rockefeller, "Magnetizing Inrush Phenomena in Transformer Banks", AIEE Transactions, vol. 77, pp. 884-892, 1958.

[90] B. Kasztenny, G. Brunello and L. Sevov, "Digital low impedance bus differential protection with reduced requirements for CTs", IEEE Transmission and distribution conference and exposition, pp. 703-708, 2001.

[91] S. Horowitz and A.G. Phadke, "Power sytem Relaying, 2nd edition", Research Studies Press LTD., 1980.

[92] S. Horowitz and Ed, "Practical Relaying for Power Systems, 2nd edition", Wiley, 1980.

[93] M. Kaufman and W. Szwander, "Busbar Protection: A Critical Review of Methods and Practice", The journal of the institution of electrical engineers, vol. 90, no. 17, 1943.

[94] S. Horowitz and A.G. Phadke, "Power sytem Relaying, 3rd edition", Research Studies Press LTD. , 2008.

[95] J. Pan, K. Vu and Y. Hu, "An efficient compensation algorithm for current transformer saturation effects", IEEE Trans. Power Deliv., vol. 19, no. 4, pp. 1623-1628, 2004.

[96] F. Haghjoo, M. Hadi Pak, "Compensation of CT distorted secondary current waveform in online conditions", IEEE Trans. Power Deliv., vol. 31, no. 2, pp. 711-720, 2016.

[97] Bogdan Kasztenny, Michael J. Thompson and Douglas Taylor, "Time-domain elements optimize the security and performance of transformer protection", 71st Annual Conference for Protective Relay Engineers (CPRE), pp. 1-15, 2018.

[98] J.O. Smith, "Mathematics of the Discrete Fourier Transform (DFT)", W3K Publishing, 2007.

[99] Feng Gao and K. Strunz, "Modeling of Constant Distributed Parameter Transmission Tine for Simulation of Natural and Envelope Waveforms in Power Electric Networks", Proceedings of the 37th Annual North American Power Symposium, pp. 247-252, 2005.

[100] EMTP reference models for transmission line relay testing, 2005.

[101] M. Kezunovic, Lj. Kojovic, A. Abur, C.W. Fromen, D.R. Sevcik and F. Phillips, "Experimental Evaluation of EMTP-Based Current Transformer Models for Protective Relay Transient Study", IEEE Trans. Power Deliv., vol. 9, no. 1, pp. 405-413, 1994.

[102] Working Group D6, Power System Relay Committee, "AC Transmission Line Model Parameter Validation", IEEE Power and Energy Society, 2014.

[103] T60 Transformer Management Relay, Instruction Manual, GE Publication, GEK-119627A, 2015.

Appendix

Table 7.1: Line Data [100]

Diameter (Inches)	R_{DC} at 50° ($\Omega/Mile$)	Earth Resitance ($\Omega - m$)
1.216	0.09222	50

Table 7.2: Tower Configuration Data [100]

Phase	Horizontal Seperation (ft)	Height at Twoer (ft)	Height at Mid Span (ft)
A	0	100	73
B	0	83.5	56.5
A	0	100	73
C	0	67	40

Table 7.3: Generator Data [100]

R_1 (Ω)	X_1 (Ω)	R_0 (Ω)	X_0 (Ω)
6.1	16.7	2.7	8.37

Table 7.4: Transformer Data

Rating	120MVA, 115kV/56kV
Configuration	YY
Z	11.6%
Magnetizing current	0.15%
Saturated flux	140%
Residual flux	90%

Table 7.5: Load Data

P	45MW
Q	21MVAR

Table 7.6: CT Excitation Data [100]

Current	Flux
0.0198	0.2851
0.0281	0.6040
0.0438	1.1141
0.0565	1.5343
0.0694	1.8607
0.1025	2.2771
0.2167	2.6522
0.7002	3.0234
1.0631	3.1098
15.903	3.2261

Vita

Monir Hossain is a PhD candidate of Electrical Engineering at University of New Orleans (UNO), LA, USA. He received his Master Degree in Electrical Engineering from University of New Orleans and Bachelor Degree from Bangladesh University of Engineering and Technology (BUET). He has more than five years of experience in power transmission engineering including protection system, and transmission system planning. Currently, he is working as a research assistant at UNO-Entergy research project on power system protection. He has published several journal and conference papers. His research interest includes power system protection and relays, energy management, and power system dynamics and oscillations.